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PoE Certification Program Test Plan

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Revision History

The following table contains a revision history for this document:

Revision	Explanation
.8	May 2nd, 2017 – Initial Draft
.85	July 25, 2017 - Editorial Revisions.
.9	July 31, 2017 – Review by Lapak, Tremblay, Calvin.
1.0	August 11, 2017 – Added final legal review content
1.1	August 29, 2017 – Removed section PSE.4.27
1.2	September 26, 2017 – Revision to PD.1.7
1.3	October 10, 2017 – Revision to PSE.1.3 (Removed/re-numberd remaining test entries)
1.4	October 19, 2017 – Revision to Clause 33 references in test overviews.
1.5	February 22, 2021 – Remove PSE Group 4 midspan tests

Product Types

The Ethernet Alliance PoE Test Plan (this document) is based on conformance verification objectives designed to demonstrate adherence to the broader set of IEEE 802.3 PoE specifications.
The intent of this program is to provide a simple and easy way to demonstrate conformance to the EA PoE Test Plan and to distinguish EA PoE products from non-conformant PoE products that are available in the marketplace today.

Testing Conditions and Requirements

Testing conditions are described in the Logo Program documentation.

Product Application Form

The Product application form must be filled out in its entirety, please see the Logo program documentation for this form.

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Detailed Test Coverage

PSE Product Testing Matrix

PSE product testing is intended to provide basic conformance assurance. The testing procedures are a reference from the UNH-IOL Clause 33 PSE Parametric Test Suite, found at the following link:
https://www.iol.unh.edu/sites/default/files/testsuites/ethernet/CL33_PSE/PSE_test_suite_v2.11.pdf and
The Clause 33 PSE Data Link Layer Classification Test Suite:
https://www.iol.unh.edu/sites/default/files/testsuites/ethernet/CL33_PSE_DLLC/PSE_DLLC_Test_Suite_v1.0.pdf

The following key describes which tests are applicable to specific product types:

Color(s)	Applies to:
	All Products
	Only Midspan Products
	Only Products which indicate support for DLL Classification

Table 1 - PSE Test Matrix

Test #	Applies to Types
Group 1: Detection Characteristics	
PSE.1.1: Valid PSE Pinout	1 & 2
PSE.1.2: Open Circuit Voltage	1 & 2
PSE.1.3: Detector Circuit Output Voltage	1 & 2
PSE.1.4: PD Signature Detection Limits	1 & 2
PSE.1.5: Physical Layer Classification	1 & 2
PSE.1.6: Physical Layer Classification Timing	1 & 2
PSE.1.7: Allowed Classification Permutations	1 & 2
PSE.1.8: New Detection Cycle	1 & 2
PSE.1.9: Alternative B Backoff Cycle	1 & 2
Group 2: Power Feed Characteristics	
PSE.2.10: Power Feed Ripple and Noise	1 & 2
PSE.2.11: Load Regulation	1 & 2
PSE.2.12: Voltage Transients	1 & 2
PSE.2.13: Power Turn On Timing	1 & 2
PSE.2.14: Apply Power	1 & 2
Group 3: Error Detection and Power Removal	
PSE.3.15: Overload Current Detection Range	1 & 2
PSE.3.16: Output Current at Short Circuit Condition	1 & 2
PSE.3.17: Output Current in Startup Mode	1 & 2
PSE.3.18: Range of TMPDO Timer	1 & 2
PSE.3.19: PD MPS Dropout Current Limits (I_{Min} measurement)	1 & 2
PSE.3.20: PD MPS Time for Validity	1 & 2
PSE.3.21: AC MPS Signal Parameters	1 & 2
PSE.3.22: AC MPS Signature	1 & 2
PSE.3.23: Turn Off Time Limits	1 & 2
Group 4: PSE Transmitter and Receiver Characteristics	1 & 2
PSE.4.24: Midspan PSE Return Loss	1 & 2 (Midspan Only)
PSE.4.25: Midspan PSE Insertion Loss	1 & 2 (Midspan Only)
GROUP 5: PSE DATA LINK LAYER CLASSIFICATION	

PSE.5.26: TLV Frame Definition	If supported
PSE.5.27: Data Link Layer Classification Timing Requirements	If supported
PSE.5.28: “PD requested power value” field changed	If supported
PSE.5.29: PSE in Sync with PD	If supported

PD Product Testing Matrix

PSE product testing is intended to provide basic conformance assurance. The testing procedures are a reference from the UNH-IOL Clause 33 PD Parametric Test Suite, found at the following link: https://www.iol.unh.edu/sites/default/files/testsuites/ethernet/CL33_PD/pd_test_suite_v2.4.pdf and The Clause 33 PD Data Link Layer Classification Test Suite: https://www.iol.unh.edu/sites/default/files/testsuites/ethernet/CL33_PD_DLLC/PD_DLLC_Test_Suite_v1.0.pdf

Color(s)	Applies to:
	All Products
	Type 2 PDs, or if support is indicated on product application sheet. Note: This testing is not required for Type 2 Evaluation Platforms

Table 2 - PD Test Matrix

Test #	Applies to Types
GROUP 1: PD ELECTRICAL CHARACTERISTICS	1 & 2
PD.1.1: Source Power	1 & 2
PD.1.2: Valid PD Pinout	1 & 2
PD.1.3: Valid Detection Signature Characteristics	1 & 2
PD.1.4: Non-Valid Detection Signature Characteristics	1 & 2
PD.1.5: Input Average Power	1 & 2
PD.1.6: PD Input Voltage	1 & 2
PD.1.7: PD Maintain Power Signature	1 & 2
PD.1.8: PD Input Inrush Current Timing (Informative)	1 & 2
PD.1.9: Peak Transient Current	1 & 2
GROUP 2: PD CLASSIFICATION TESTS	
PD.2.10: Allowed Classification Permutations	1 & 2
PD.2.11: Single Event Physical Layer Classification	1 & 2
PD.2.12: Two Event Physical Layer Classification	1 & 2
PD.2.13: Classification Stability Time	1 & 2
GROUP 3: PD DATA LINK LAYER CLASSIFICATION	
PD.3.14: TLV Frame Definition	2 or Type 1 if supported
PD.3.15: Set pd_dll_ready	2 or Type 1 if supported
PD.3.16: “PSE allocated power value” field changed	2 or Type 1 if supported
PD.3.17: PD in Sync with PSE	2 or Type 1 if supported

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PSE Tests

Group 1: Detection Characteristics

Scope: This group of tests verifies the electrical and functional characteristics during the detection mode of Power Sourcing Equipment.

Overview: These tests apply to IEEE Std 802.3-2015 Clause 33 PoE devices. Specifically, the problems related to the functional and electrical characteristics of Power Sourcing Equipment's detection sequence.

PSE.1.1: Valid PSE Pinout

Purpose: To verify that pinout of the Power Sourcing Equipment is valid.

References:
[1] IEEE Std 802.3-2015: Subclause 33.2.1, Figures 33–4, 33–5, 33–6, 33–7, Table 33–2.
[2] IEEE Std 802.3-2015: Subclause 33.8.3.2, Items PSE1, PSE2
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.1.1

Discussion: A PSE can be located with or on a link segment that is separate from the DTE/Repeater; these two locations are known as Endpoint PSE and Midspan PSE respectively. Regardless of the PSE location, detection and power can be applied with either Alternative A or Alternative B pinouts. These pinouts are defined in the Table 33–2, reprinted below.

Conductor	Alternative A (MDI-X)	Alternative A (MDI)	Alternative B (All)
1	Negative V_{Port}	Positive V_{Port}	
2	Negative V_{Port}	Positive V_{Port}	
3	Positive V_{Port}	Negative V_{Port}	
4			Positive V_{Port}
5			Positive V_{Port}
6	Positive V_{Port}	Negative V_{Port}	
7			Negative V_{Port}
8			Negative V_{Port}

Table 33–2 – PSE pinout alternatives

Test Setup: The DUT is connected to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
1. Determine the Location of the PSE, Endpoint or Midspan.
2. Connect the Test Equipment using Alternative A.
3. Attempt to power the Test Equipment.
4. Switch Alternative and repeat steps 1–2.

Observable Results:
The DUT should implement the correct pinout given its location on the link segment.

Possible Problems: None

PSE.1.2: Open Circuit Voltage

Purpose: To verify that the open circuit voltage at the PI of the PSE during detection mode is below the conformance limit.

References:
[1] IEEE Std 802.3-2015: Subclause 33.2.5.1 and Table 33–4.
[2] IEEE Std 802.3-2015: Subclause 33.8.3.2, Item PSE13
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.1.2

Discussion: During the detection mode, the open circuit voltage (V_{OC}) of the PSE should not exceed 30V.

Test Setup: The DUT is connected to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
1. Measure the open circuit voltage at the PI of the DUT using a high impedance probe.

Observable Results:
V_{OC} (the open circuit voltage) should not exceed 30 Volts.

Possible Problems: None

PSE.1.3: Detector Circuit Output Voltage

Purpose: To verify that the test voltages of the PSE detection circuit conform to the specifications defined in Table 33–4.

References:
[1] IEEE Std 802.3-2015: Subclause 33.2.5.2, Table 33–4
[2] IEEE Std 802.3-2015: Subclause 33.8.3.2, Items PSE17, PSE18, PSE19
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.1.6

Discussion: While the PSE is probing the link segment for a valid PD detection signature, the detection voltage V_{detect} at the PSE PI should be within the V_{valid} voltage range of 2.8 to 10 Volts. The loaded circuit values are measured with a valid PD signature attached to the PSE. The PSE should make at least 2 measurements with V_{detect} values that create at least a ΔV_{test} difference of 1 Volt.

Test Setup: The DUT is connected to the Test Equipment with a short cable (approximately 1m in length). Confirm that the DUT is operating in PD detection mode and transmitting probe voltages.

Procedure:
1. Supply a valid signature using the Test Equipment board at the PI of the DUT.
2. Measure the probe voltages at the PI of the DUT.
3. Measure the slew rate of the probe voltages.

Observable Results:
In step 2, V_{VALID} (the loaded PI output detection voltages) should be between 2.8 and 10 volts.
In step 2, ΔV_{TEST} should be at least 1 volt.
In step 3, V_{SLEW} (the slew rate of the probe voltages) should be less than 0.1 V/µs

Possible Problems: None

PSE.1.4: PD Signature Detection Limits

Purpose: To verify that the DUT will properly detect a PD's signature impedance.

References:
[1] IEEE Std 802.3-2015: Subclause 33.2.5.3; Subclause 33.2.5.4; Table 33–5, Table 33-6.
[2] IEEE Std 802.3-2015: Subclause 33.8.3.2, Items PSE29, PSE20
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.1.8

Discussion: The PSE should detect a valid signature for a link segment that has the characteristics of R_{good} and C_{good} between the powering pairs. The PSE should detect an invalid signature for a link segment that has the characteristics of R_{bad} and C_{bad} between the powering pairs. The PSE should only provide power if the PD presents a valid signature which is compliant with Table 33–5 and Table 33-6 which are synthesized here for convenience.

Item	Parameter	Minimum	Maximum
7	R_{good} (KΩ)	19.0	26.5
8	R_{bad} (KΩ)	15.0	33
10	C_{good} (nF)		150
11	C_{bad} (µF)	10.0	

Table 33–5 and 33–6

Test Setup: The DUT is connected to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
Part a: Input Resistance Minimums

1. Adjust the Test Equipment to have a valid input signature capacitance (0.1µF).
2. Increase the signature resistance from Rbadmin until the DUT supplies power to the PD.
3. Record the value at which the PSE accepts the PD signature resistance.
4. Decrease the signature resistance below Rgoodmin until the DUT does not supply power to the PD.
5. Record the value at which the PSE rejects the PD signature resistance.

Part b: Input Resistance Maximums

6. Increase the signature resistance above Rgoodmax until the DUT does not supply power to the PD.
7. Record the value at which the PSE rejects the PD signature resistance.
8. Decrease the signature resistance from Rbadmax until the DUT supplies power to the PD.
9. Record the value at which the PSE accepts the PD signature resistance.

Part c: Input Capacitance "Must Accept"

10. Set the PD signature model to have a resistance between Rgoodmin and Rgoodmax (25kΩ).
11. Set the PD signature model to have a capacitance of Csigmax less than 150nF.
12. Connect the PD signature model to the PI of the DUT and observe the voltage at the PI.

Part d: Input Capacitance "Must Reject"

13. Set the PD signature model to have a capacitance of greater than Cbadmin (10 µF).
14. Connect the PD signature model to the PI of the DUT and observe the voltage at the PI.

Observable Results:

In step 3 and 5, $R_{accept(min)}$ should be between 15kΩ and 19kΩ
In step 7 and 9, $R_{accept(max)}$ should be between 26.5kΩ and 33kΩ
In step 12, the DUT should accept the PD signature and should provide power
In step 14, the DUT should reject the PD signature and should not provide power

Possible Problems: None.

PSE.1.5: Physical Layer Classification

Purpose: To verify a PSE supporting classification properly performs PD classification detection.

Reference:
[1] IEEE Std 802.3-2015: Subclause 33.2.6.1, Table 33–7, Table 33–9.
[2] IEEE Std 802.3-2015: Subclause 33.8.3.2, Items PSE25, PSE26, PSE27, PSE28, PSE29, PSE31
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.1.9

Discussion: The PSE may attempt to classify the PD. Also, the PD may provide information to allow features such as load management to be implemented. For a PSE that performs 1-event classification, the PSE should probe the PD with a voltage between 15.5 and 20.5 volts limited to 100mA. A PSE that performs 2-event classification must present two class events in the 15.5 to 20.5 Volt range separated by a mark event of 7 to 10 Volts. The class events are limited to 100mA, and the mark event is limited to the range of 5mA to 100mA. The PSE should measure I_{Class} and classify the PD based on the observed current as dictated by Table 33–9, which is printed here for convenience.

Measure I_{class}	**Classification**
0mA to 5.00mA	Class 0
>5.00mA and <8.00ma	May be Class 0 or 1
8.00mA to 13.0mA	Class1
>13.0mA and <16.0mA	May be Class 0,1 or 2
16.0mA to 21.0mA	Class 2
>21.0mA and <25.0mA	May be Class 0,2 or 3
25.0mA to 31.0mA	Class 3
>31.0mA and <35.0mA	May be Class 0,3 or 4
35.0mA to 45.0mA	Class 4
>45.0mA and <51.0mA	May be Class 0 or 4

Table 33–9

Test Setup: The DUT is connected to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
1. Configure the Test Equipment to draw Class 0 currents.
2. Measure classification sequence voltages using an oscilloscope.
3. Determine the observed classification level through the management of the DUT.
4. Repeat steps 1-3 for Class 0 through Class 4.
5. Configure the Test Equipment to draw 150mA Class current.
6. Measure the $I_{CLASS-LIM}$.
7. Determine the observed classification level through the management of the DUT.

Observable Results:
In step 2, there should be one class pulse, $V_{CLASS,}$ which should be between 15.5 and 20.5 Volts.
In step2, for class 4 current draws a 2-Event classification DUT, should provide two class pulses of V_{CLASS} between 15.5 and 20.5 Volts. They should be separated by V_{Mark}, which should be between 7 and 10 volts.
In step 3, the DUT should accurately classify the PD.
In step 7, if the current drawn is equal to or greater than 51mA, a Type 1 PSE shall either return to the IDLE state or classify the PD as Class 0; a Type 2 PSE shall return to the IDLE state.
In step 6, I_{CLASS_LIM} should be between 51 and 100mA for both Type 1 and Type 2 PSEs. I_{MARK_LIM} should be between 5 and 100mA for all mark events.

Possible Problems: If the DUT does not perform classification, then the DUT should assign the PD to Class 0**.**

PSE.1.6: Physical Layer Classification Timing

Purpose: To verify that a PSE capable of classifying a PD performs classifications within the specified timing constraints.

References:
[1] IEEE Std 802.3-2015: Subclause 33.2.6.1, Table 33–10
[2] IEEE Std 802.3-2015: Subclause 33.8.3.2, Items PSE4, PSE30, PSE32
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.1.10

Discussion: After successful detection of a PD, a PSE supporting 1-event classification must complete classification within 6 to 75ms (T_{pdc}). For a PSE that supports 2-event classification, each of the two class events (T_{CLE1} and T_{CLE2}) should complete within 6 to 30ms. Following the first class event, the first mark event (T_{ME1}) should complete within 6 to 12ms. Following the second class event, a second mark event (T_{ME2}) occurs that must endure for a period exceeding 6ms. Classification should complete within 400 ms after completion of detection (T_{pon}). If the PSE fails to power the PD within T_{pon}, it must reinitiate detection prior to power up.

Test Setup: The DUT is connected to the Test Equipment with a short cable (approximately 1m in length)..

Procedure:
1. Measure the length of the classification pulses.

Observable Results:
For 1-event classification the T_{PDC} should be between 6 and 75ms.
For 2-event classification T_{CLE1} and T_{CLE2} should be between 6 and 30ms.
For 2-event classification, T_{ME1} should be between 6 and 12ms.
For 2-event classification, T_{ME2} should be greater than 6ms.

Possible Problems: This test does not apply to a DUT that does not perform PD classification.

PSE.1.7: Allowed Classification Permutations

Purpose: To verify whether the PSE fits a valid classification permutation.

References:
[1] IEEE Std 802.3-2015: Subclause 33.2.6, Table 33–8
[2] IEEE Std 802.3-2015: Subclause 33.8.3.2, Item PSE21
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.1.11

Discussion: A PSE shall meet one of the allowable classification permutations in Table 33–8.

Permutations			PSE allowed?	PD allowed?
PSE/PD Type	Physical Layer classification	Data Link Layer classification		
Type 2	2-Event	No	Yes	No
		Yes	Yes	Yes
	1-Event	No	No	No
		Yes	Yes	No
	None	No	No	No
		Yes	No	No
Type 1	2-Event	No	No	Yes
		Yes	No	Yes
	1-Event	No	Yes	Yes
		Yes	Yes	Yes
	None	No	Yes	No
		Yes	Yes	No

Table 33-8

Test Setup: The DUT is connected to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
1. Based on the classification voltage waveform determine whether the PSE is using a 1-Event or a 2-Event Physical Layer classification.
2. Monitor Network Activity for several minutes to determine whether the DUT is utilizing Data Link Layer Classification.
3. If Data Link Layer Classification is observed, request maximum power with Data Link Layer Classification.
4. Determine the PSE Type by observing the maximum power available at the PI.

Observable Results:
The DUT should be an allowable type as specified by table 33-8

Possible Problems: None.

PSE.1.8: New Detection Cycle

Purpose: To verify that if the PSE is unable to supply power within T_{pon} then, it initiates and successfully completes a new detection cycle before powering on.

References:
[1] IEEE Std 802.3-2015: Subclause 33.2.4.1, Table 33–11.
[2] IEEE Std 802.3-2015: Subclause 33.8.3.2, Items PSE4, PSE19
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.1.12

Discussion: The PSE may apply power after a valid sequence of detection and optional classification. However if the PSE is unable to supply power within a time interval of 400ms (tpon_timer), then it must initiate a new valid detection cycle before applying power. The 'tpon_timer' timer is used to limit the time for power turn-on, which is referred to as T_{pon} in Table 33–11.

Test Setup: The DUT is connected to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
1. Supply a valid signature at the DUT's PI for a time approximately lesser than the T_{pon} of the DUT. (Refer to Test # 33.1.7 for the value of turn on time for the DUT.)
2. Connect an invalid signature at the DUT's PI for at least 2sec.
3. Reconnect the valid signature at the DUT's PI.
4. Observe the waveform on the oscilloscope.
5. Measure the detection time.
6. Measure T_{pon}.

Observable Results:
The DUT should complete a full detection cycle before applying power to the Test Equipment.

Possible Problems: None

PSE.1.9: Alternative B Backoff Cycle

Purpose: To verify that if a PSE that implements Alternative B fails to detect a valid detection signature at its PI, it will back off for no less than T_{dbo} and apply a voltage V_{off} less than 2.8VDC during the backoff.

References:
[1] IEEE Std 802.3-2015: Subclause 33.2.4.1, Table 33–11.
[2] IEEE Std 802.3-2015: Subclause 33.8.3.2, Item PSE5
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.1.13

Discussion: A PSE that implements Alternative B will start the 'tdbo_timer' if it fails to detect a valid signature at its PI. The 'tdbo_timer' is used to regulate backoff upon detection of an invalid signature as is referred to as T_{dbo} in Table 33–11. During this backoff period, the PSE must not apply a voltage V_{off} greater than 2.8Vdc to the PI. A PSE that implements Alternative B detection must not resume detection mode until at least one backoff cycle has elapsed.

Test Setup: The PSE is connected to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
1. Connect an invalid signature at the DUT's PI.
2. Measure the DC voltage between the consecutive valid detection sequences.
3. Measure the time between consecutive valid detection sequences.

Observable Results:
In step 2, the DUT must not apply a voltage V_{off} greater than 2.8 Vdc at its PI.
In step 3, $T_{dbo} > 2$ sec.

Possible Problems: This test does not apply to a PSE that implements Alternative A.

Group 2: Power Feed Characteristics

Scope: This group of tests verifies the electrical and functional characteristics during of the Power Sourcing Equipment while feeding power.

Overview: These tests apply to IEEE Std 802.3-2015 Clause 33 PoE devices. Specifically, the problems related to the functional and electrical characteristics of Power Sourcing Equipment.

PSE.2.10: Power Feed Ripple and Noise

Purpose: To verify the power feeding ripple and noise are within the conformance limits.

References:
[1] IEEE Std 802.3at™-2009: Subclause 33.2.7.3, Table 33–11
[2] IEEE Std 802.3-2015: Subclause 33.8.3.2, Item PSE52
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.2.1

Discussion: The PSE should source power at all rated levels with noise and ripple that are below the levels specified in Table 33–11 (printed here for convenience). Excessive noise may cause attached PDs to behave abnormally.

Parameter	Min	Max
Power feeding Ripple and noise (Vpp)		
f < 500Hz		0.50
500Hz ≤ f < 150KHz		0.20
150KHz ≤ f < 500KHz		0.15

Table 33–11

Test Setup: The DUT is connected to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
1. Adjust the PD to sink .44 watts.
2. Measure the amount of pair-to-pair ripple and noise voltage at the PI of the PSE.
3. Measure the amount of common-mode ripple and noise voltage at the PI of the PSE.
4. Adjust the PD to sink maximum allowable power.
5. Repeat steps 3 and 4.

Observable Results:
The ripple and noise peak-to-peak voltages, pair-to-pair and common-mode, in the band 0-500Hz will be less than 0.50 volts.
The ripple and noise peak-to-peak voltages, pair-to-pair and common-mode, in the band 500Hz-150kHz will be less than 0.20 volts.
The ripple and noise peak-to-peak voltages, pair-to-pair and common-mode, in the band 150kHz-500kHz will be less than 0.15 volts.

PSE.2.11: Load Regulation

Purpose: To verify that the PSE performs load regulation while supplying power on its PI.

References:
[1] IEEE Std 802.3-2015: Subclause 33.2.7.1, Table 33–11
[2] IEEE Std 802.3-2015: Subclause 33.8.3.2, Item PSE48
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.2.2

Discussion: The PSE should perform voltage regulation while supplying power to a PD over the PI. The output voltage of the PSE must stay between 44 and 57 volts for a Type 1 product or 50 to 57 volts for a Type 2 product while the load changes at a rate of 15 to 35mA/µs. The PSE must not produce any transients greater than 3.5V/µs. These requirements prevent the voltage supply from exceeding the operating range of a PD.

Test Setup: Connect the DUT to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
1. Connect the PSE to the Test Equipment with a valid signature and the load set to draw 10mA.
2. For a Type 1 product, rapidly adjust the current draw of the PD from 10mA to 350mA. This transition needs to occur within 340 / 35 µs (approximately 9.7 µs) to 340 / 15 µs (approximately 22.7µs).
   For a type 2 product, rapidly adjust the current draw of the PD from 10mA to 600mA. This transition needs to occur within 590 / 35 µs (approximately 16.9 µs) to 590 / 15 µs (approximately 39.3µs)
3. Observe the voltage transients and output voltage of the PSE at the PI.

Observable Results:
In step 3, the voltage transients seen should not exceed 3.5V/µs.
In step 3, the DUT output voltage at the PI should be within the range of 44 to 57 volts for a Type 1 product or 50 to 57 volts for a Type 2 product.

Possible Problems: None.

PSE.2.12: Voltage Transients

Purpose: To verify that the Type 2 PSE maintains proper output voltages for transient conditions.

References:
[1] IEEE Std 802.3-2015: Subclause 33.2.7.2, Table 33–49
[2] IEEE Std 802.3-2015: Subclause 33.8.3.2, Items PSE57, PSE58, PSE59
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.2.3

Discussion: The Type 2 PSE must maintain an output voltage that varies by less than K_{trans_lo} below V_{port}min for transient conditions lasting between 30 to 250µs. Transients lasting more than 250µs should meet the static V_{port} specification.

Test Setup: The DUT is connected to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
1. Confirm that the detection of the PD has been successfully completed.
2. Apply transients between 30 and 250µs and measure V_{port}.
3. Apply transients above 250µs and measure V_{port}.

Observable results:
For a Type-2 PSE, V_{PORT} should not go below 46.2 Volts for any transient between 30 and 250µs. V_{PORT} should not go below 50V for any transient lasting more than 250µs

Possible Problems: This test only applies to Type 2 PSEs. A Type 2 PSE may remove power from the PI if V_{port} is below 50V.

PSE.2.13: Power Turn On Timing

Purpose: To verify that the PSE starts applying power within T_{pon} after it has successfully detected the PD.

References:
[1] IEEE Std 802.3-2015: Subclause 33.2.7.12, Table 33–11
[2] IEEE Std 802.3-2015: Subclause 33.8.3.2, Items PSE4, PSE9
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.2.4

Discussion: The PSE must power on the PD after detection within T_{pon}. If the PSE fails to power the PD within 400ms (T_{pon}), it must reinitiate the detection sequence.

Test Setup: The DUT is connected to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
1. Confirm that the detection of the PD has been successfully completed.
2. Measure the time delay between the end of detection and when the PSE starts applying power.

Observable results:
In step 2, T_{pon} should not be greater than 400ms.

Possible Problems: None.

PSE.2.14: Apply Power

Purpose: To verify that the PSE applies power on the same pairs as those used for detection after completing a valid detection.

References:
[1] IEEE Std 802.3-2015: Subclause 33.2.5, Table 33-11
[2] IEEE Std 802.3-2015: Subclause 33.8.3.2, Items PSE9, PSE10
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.2.5

Discussion: A PSE detects the PD by probing it via the PSE's PI. A PSE should apply power only after it has completed the detection of a PD. The power should be supplied on the same pairs as those used for detection.

Test Setup: The DUT is connected to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
1. Supply a valid signature at the DUT's PI for a time approximately equal to T_{det} of the DUT.
2. Confirm that the DUT performs valid detection sequence before powering the PD simulator.
3. Check the pairs on which DUT supplies power.

Observable Results:
In step 2, the DUT must power the Test Equipment only after a proper detection sequence.
In step 3, the DUT should supply power on the same pairs as that it performed detection for the Test Equipment.

Possible Problems: None

Group 3: Error Detection and Power Removal

Scope: This group of tests verifies the electrical and functional characteristics during error detection and power removal.

Overview: These tests apply to IEEE Std 802.3-2015 Clause 33 PoE devices. Specifically, the problems related to the functional and electrical characteristics of Power Sourcing Equipment.

PSE.3.15: Overload Current Detection Range

Purpose: To verify that I_{CUT} is within the specified limits.

References:
[1] IEEE Std 802.3-2015: Subclause 33.2.7.6, Table 33–11
[2] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.3.1

Discussion: The PSE monitors the current (I_{Port}) drawn by the PD. If I_{Port} exceeds the overload current detection range I_{CUT} for greater than 75ms (T_{ovld}), the PSE should remove power from its PI. I_{CUT} has a minimum value of P_{Class}/V_{Port} and a Type 1 maximum of 400mA or a Type 2 maximum of (400/350)*(P_{Port}/V_{Port}). This is an optional specification.

Test Setup: The DUT is connected to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
1. Verify that the PD is drawing current greater than or equal to I_{Min} from the DUT.
2. Measure the V_{Port} at the PI of the PSE.
3. Decrease the load resistance gradually until the DUT removes power from its PI.
4. Measure the current (I_{CUT}) at which the DUT stops supplying power.

Observable Results:
For Type 1 PSEs, I_{CUT} should be between P_{Class}/V_{Port} and 400mA
For Type 2 PSEs, I_{CUT} should be between P_{Class}/V_{Port} and (400/350)*(P_{Port}/V_{Port})

Possible Problems: None

PSE.3.16: Output Current at Short Circuit Condition

Purpose: To verify that the output current at short circuit condition falls within the specified amplitude and timing.

References:
[1] IEEE Std 802.3-2015: Subclause 33.2.7.7, Table 33–1, Table 33-11, Figure 33-14
[2] IEEE Std 802.3-2015: Subclause 33.8.3.2, Items PSE56, PSE57, PSE58
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.3.3

Discussion: The PSE monitors the current (I_{Port}) drawn by the PD at the PI. If I_{Port} meets or exceeds the "PSE lowerbound template", the PSE should remove power from its PI. The PSE should remove power before the current exceeds the "PSE upperbound template" in Figure 33-14 reprinted below for convenience.

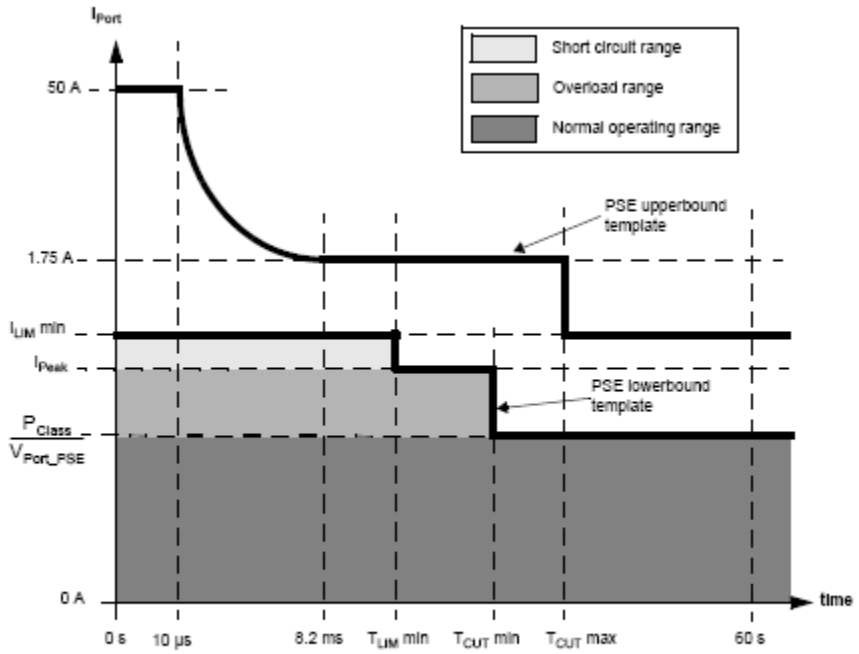


Figure 33–14—POWER_ON state PI operating current templates

Test Setup: The DUT is connected to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
1. Verify that the PSE is powered and outside of startup mode.
2. Apply a load that violates the "PSE upperbound template".
3. Measure the resulting current draw.
4. Repeat steps 1-3 with different current draws that violate the PSE upperbound template.
5. Confirm that the DUT does not remove power when below the PSE lowerbound template.

Observable Results:
In step 3, the DUT should limit I_{PORT} when it exceeds the PSE upperbound template.
In step 5, the DUT should not remove power when below the PSE lowerbound template.

Possible Problems: In step 2, it is possible that the PSE will limit the current draw at the PI, and thus drawing certain currents along the upperbound template may not be possible. The PSE may also remove power if the voltage

at the PI decreases below a normal V_{port} range. This behavior is still conformant, but may also prohibit testing certain currents in the upperbound template.

PSE.3.17: Output Current in Startup Mode

Purpose: To verify that the inrush current during startup conforms to the specified values. Also, to ensure the PSE removes power within the conformant time limit when it detects a short circuit condition.

References:
[1] IEEE Std 802.3-2015: Subclause 33.2.7.5, Table 33–11, Figure 33-13
[2] IEEE Std 802.3-2015: Subclause 33.8.3.2, Item PSE54, PSE55
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.3.4

Discussion: The standard defines the output current, I_{INRUSH}, in startup mode. Startup mode is defined as the transition to the POWER_UP state to the lesser of T_{INRUSH} or the conclusion of the PD inrush currents. During startup, for PI voltages above 30 V, the minimum I_{INRUSH} requirement is 400mA. The whole process is limited by T_{INRUSH}, which is limited between 50 and 75 ms. Also, all of the measurements must be taken after 1ms to ignore startup transients. See Figure 33-13.

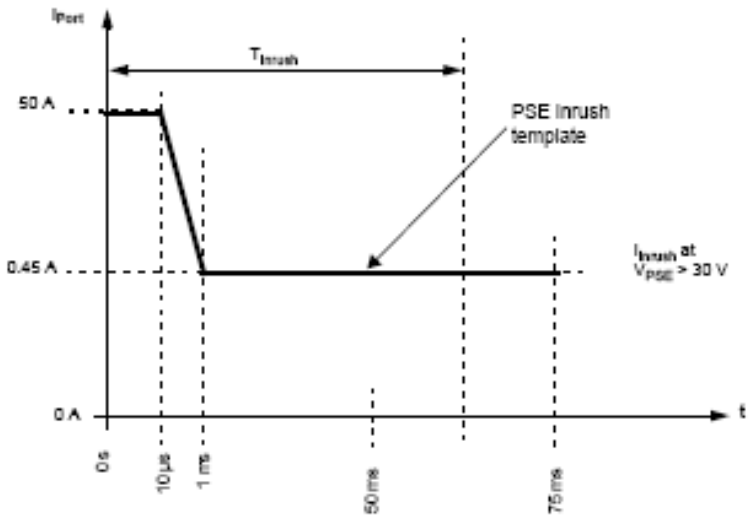


Figure 33–13—I_{Inrush} current and timing limits in POWER_UP state

Test Setup: The DUT is connected to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
1. Configure Test Equipment to short when voltages are above 40 Volts.
2. Allow DUT to power up.
3. Measure resulting current waveform.
4. Repeat for 31V.

Observable Results:
In step 3 for voltages above 30V, I_{INRUSH} should be between 400mA and 450mA (inclusive).
In step 3, all waveforms must be between 50ms and 75ms (inclusive)

Possible Problems: Shorting the DUT for voltages in the detection and classification range may cause improper detection and/or classification.

PSE.3.18: Range of TMPDO Timer

Purpose: To verify that the PSE correctly monitors the PD Maintain Power Signature.

References:
[1] IEEE Std 802.3-2015: Subclause 33.2.9.1.1, Subclause 33.2.9.1.2 Table 33–11, Figure 33–9, Figure 33–12.
[2] IEEE Std 802.3-2015: Subclause 33.8.3.2, Item PSE65, PSE68
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.3.6

Discussion: Once a PSE has entered the 'POWER_ON' state, it must receive an 'mr_mps_valid' from the link partner within a specified amount of time. If this message is not received, it will enter the 'IDLE_MPS' state and remove power from the link segment before attempting a new detection sequence. This time is defined by the product's 'tmpdo_timer' and is required to be between 300ms and 400ms. This test is designed to verify that the product under test enters the 'IDLE_MPS' state from the 'POWER_ON' state when an mr_mps_valid message is not received from its link partner in the acceptable range of time.

Test Setup: The DUT is connected to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
Part a: DC disconnect
1. Attach a valid signature to the PI of the DUT such that the DUT enters the 'POWER_ON' state.
2. Reduce the current drawn by the PD to 2mA for t ≤ 300ms.
3. Observe whether the DUT entered the 'IDLE_MPS' state.
4. Repeat steps 1–3 varying t until the DUT enters the 'IDLE_MPS' state.
5. Find the t for which the PSE removes power.

Part b: AC disconnect
6. Attach a valid signature to the PI of the DUT such that the DUT enters the 'POWER ON' state.
7. Disconnect the PD from the PI of the DUT.
8. Measure the time taken by the DUT to remove power.

Observable Results:
Part a:
In step 5, verify that 300ms ≤ T_{MPDO} ≤ 400 ms.
Part b:
In step 8, verify that 300 ms ≤ T_{MPDO} ≤ 400 ms.

Possible Problems: None.

PSE.3.19: PD MPS Dropout Current Limits (I_{Min} measurement)

Purpose: To verify that the PSE correctly monitors the PD Maintain Power Signature.

References:
[1] IEEE Std 802.3-2015: Subclause 33.2.9.1.2, Table 33–11
[2] IEEE Std 802.3-2015: Subclause 33.8.3.2, Item PSE66, PSE69
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.3.7

Discussion: The PSE must monitor the link segment for the PD's Maintain Power Signature, and remove power if it detects that the PD is disconnected. The PSE may monitor the AC MPS component, the DC MPS component, or both signature components. If the PSE monitors the DC MPS component, the DUT should remove power from the PI if the current drawn by the PD drops below 5mA ($I_{MIN1\ (max)}$) for more than 400 ms (T_{MPDO}). The PSE may remove power if the current drawn by the PD is between 5mA and 10mA($I_{MIN2\ (max)}$) for greater than 400ms(T_{MPDO}).

Test Setup: The DUT is connected to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
1. Set the Test Equipment to draw 10mA of current from the DUT.
2. Decrease the current draw of the Test Equipment from 10mA to less than 5mA for 400ms, in steps of 0.1mA.
3. Observe the output voltage at the PI of the DUT during each step.
4. Record the current draw at which the PSE removes power.

Observable Results:
In Step 4, if the current drawn by the Test Equipment is between 5mA and 10mA, the DUT may disconnect power from the PI.
In Step 4, if the current drawn by the Test Equipment is less than 5mA, the DUT must disconnect power from the PI.

Possible Problems: This test does not apply if the DUT performs only AC disconnect.

PSE.3.20: PD MPS Time for Validity

Purpose: To verify that the PSE waits for at least the minimum MPS validity time when it monitors the DC MPS component.

References:
[1] IEEE Std 802.3-2015: Subclause33.2.9, Table 33–11
[2] IEEE Std 802.3-2015: Subclause 33.8.3.2, Item PSE70
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.3.8

Discussion: The PSE can monitor either the DC or AC MPS component to verify if the PD is still drawing the minimum current (I_{MIN2}) that is required by the PSE. A PSE that monitors the DC MPS component of the signature will remove power from its PI if it detects that the PD is drawing current less than its I_{MIN1} (5mA) for greater than 400ms. In order to maintain a valid MPS signature, the PD can draw less than the I_{MIN1} (5mA) for 300ms and then draw more than its I_{MIN2} max (10mA) for the next 60ms(T_{MPS}) or more. This improves the power efficiency of the PSE.

Test Setup: The DUT is connected to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
1. Verify that the DUT is supplying power to the Test Equipment.
2. Confirm that the Test Equipment is drawing more than 10 mA.
3. Set the Test Equipment to draw more than 10 mA for a period of 60ms (T_{MPS}) and then drop the current back to less than 5 mA for the next 300ms. Cycle this sequence.
4. Confirm that the DUT does not remove power from the PI.

Observable Results:
In step 4, for $T_{MPS} \geq$ 60ms the DUT does not remove power.

Possible Problems: If the DUT does not support DC MPS, then this test does not apply.

PSE.3.21: AC MPS Signal Parameters

Purpose: To verify that the PI AC probing signals fall within the conformance limits.

References:
[1] IEEE Std 802.3-2015: Subclause 33.2.9.1 Table 33–12, Figure 33C.15.
[2] IEEE Std 802.3-2015: Subclause 33.8.3.2, Items PSE64
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.3.9

Discussion: Once power has been applied to the link section, the PSE must monitor the link segment for the PD's Maintain Power Signature, and remove power if it detects that the PD has been disconnected. The PSE may monitor the AC MPS component, the DC MPS component, or both signature components. This test has been designed to verify that a PSE that monitors the AC MPS component meets the AC signal parameters as specified in Item 1(a-c) of Table 33–12, which has been printed here for convenience. These parameters can be measured as depicted in Figure 33C.15, which is also printed here for convenience.

Item	Parameter		Min	Max
	AC Signal Parameters			
1a	PI probing AC Voltage	V_open (Vpp)	1.9	10% of the average value of VPort within the limits of Table 33–11, item 1
		V_open1 (Vp)		30V, VPort≤44V
1b	AC Probing Signal Frequency	Fp (Hz)		500
1c	AC Probing Signal Slew Rate	SR (V/µs)		0.1 (Positive or negative)

Table 33–12

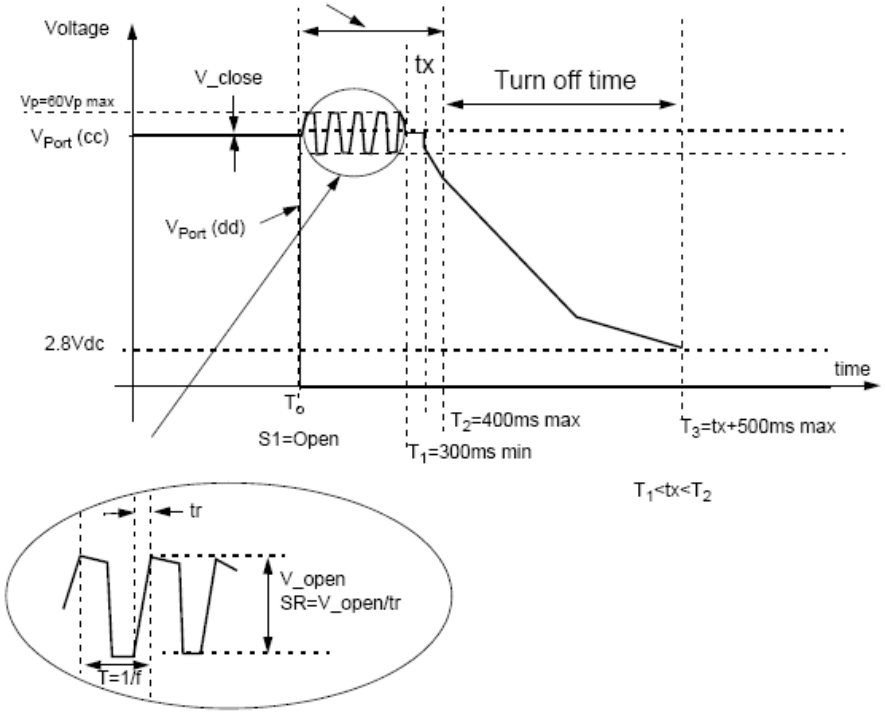


Figure 33C.15

Test Setup: The DUT is connected to the Test Equipment with a short cable (approximately 1m in length).

Procedure:

1. Attach a valid signature (less than or equal to 27KΩ) to the PI of the DUT.
2. Verify that the DUT is supplying power to the Test Equipment.
3. Disconnect the signature from the PI of the DUT.
4. Measure the PI probing AC voltage (V_open).
5. Measure the PI probing signal frequency.
6. Compute the AC probing signal slew rate (SR).
7. Measure the peak value (Vp).

Observable Results:
1.9V ≤V_open ≤10% of average value of V_{port} (44V <V_{Port} <57V).
The PI probing frequency should not be greater than 500Hz.
The slew rate should not be greater than 0.1V/µs.
The peak value (Vp) should be less than 60Volts

Possible Problems: If the DUT does not support AC MPS, then this test does not apply.

PSE.3.22: AC MPS Signature

Purpose: To verify that the PSE that implements AC MPS component correctly monitors the PD Maintain Power Signature.

References:
[1] IEEE Std 802.3-2015: Subclause 33.2.9.1.1 Table 33–12, Figure 33–15, Figure33–16.
[2] IEEE Std 802.3-2015: Subclause 33.8.3.2, Item PSE64, PSE65
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.3.10

Discussion: The PSE must monitor the link segment for the PD's Maintain Power Signature, and remove power if it detects that the PD is disconnected. The PSE may monitor the AC MPS component, the DC MPS component, or both signature components. A PSE that monitors AC MPS component will remove power it if detects an AC impedance at the PI equal to or greater than 1980 KΩ (|Zac2|) as defined in Table 33–12, which is printed below for convenience. It may or may not remove power if it detects an AC impedance between 27KΩ (|Zac1|) and |Zac2|. The PSE will maintain power if it detects an impendence less than or equal to |Zac1|. The PSE will remove power from its PI if the AC MPS signature is absent for more than 400ms (T_{MPDO}).

Item	Parameter	Symbol	Unit	Min	Max	Additional information
	AC Maintain Power Signature					
4a	Shall not remove power from the PI	$\lvert Z_{ac1} \rvert$	KΩ		27	F_p= 5Hz, Testing voltage >2.5V. See Figure 33–16. Impedance shall have non- negative resistive compo- nent and a net capacitive reactive component.
4b	Shall remove power from the PI	$\lvert Z_{ac2} \rvert$	KΩ	1980		See Figure 33–17.

Table 33–12

Test Setup: The DUT is connected to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
1. Allow the DUT to deliver power and supply a valid current draw.
2. Place an impedance in the Zac1 range across the PI.
3. Remove the valid current draw and confirm that the DUT is still powering.
4. Repeat steps 2 and 3 for multiple values across the Zac1 range.
5. Place an impedance of 27KΩ across the PI.
6. Repeat steps 3 and 5 increasing the impedance until the DUT disconnects.

Observable Results:
In Step 3, the DUT should supply power onto its PI.
In Step 6, the impedance (Z) should be between 27KΩ and 1980KΩ (inclusive).

Possible Problems: If the DUT does not implement AC MPS disconnect, then this test does not apply.

PSE.3.23: Turn Off Time Limits

Purpose: To verify that the PSE disconnects power within T_{Off} through a test resistor.

References:
[1] IEEE Std 802.3-2015: Subclause 33.2.7.8, 33.2.9.1, Table 33–11
[2] IEEE Std 802.3-2015: Subclause 33.8.3.2, Item PSE59
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.3.11

Discussion: When the DUT is disconnected from a valid maintain power signature it should remove power within T_{Off} through a test resistor of 320kΩ attached to the PI. T_{Off} is defined as the discharge time from 1 Volt less than static V_{Port} to 2.8Vdc.

Test Setup: The DUT is connected to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
1. Verify that the DUT is supplying power to the Test Equipment.
2. Disconnect DUT with a 320kΩ test resistor attached to the PI.
3. Measure the discharge time when the DUT removes power from its PI.

Observable Results:
In step 3, $T_{Off} \leq 500ms$.

Possible Problems: For AC MPS the DUT can observe the test resistor as a valid MPS and will remain in powering mode.

Group 4: PSE Transmitter and Receiver Characteristics

Scope: This group of tests deals with conformance parameters specific to the transmitter and receiver of a PSE.

Overview: These tests apply to IEEE Std 802.3-2015 Clause 33 PoE devices. Specifically, the problems related to the functional and electrical characteristics of Power Sourcing Equipment products.

PSE.4.24: Midspan PSE Return Loss

Purpose: To verify that the return loss of a Midspan PSE is greater than the minimum conformant value.

References:
[1] IEEE Std 802.3-2015: Subclause 33.4.9.1.3, Table 33–20.
[2] IEEE Std 802.3-2015: Subclause 33.8.3.4 Item PSEEL12, Subclause 33.8.3.5 Item PSEEL11
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.4.1

This test is no longer required.

PSE.4.25: Midspan PSE Insertion Loss

Purpose: To verify that the insertion loss of a Midspan PSE is less than the maximum conformant value.

References:
[1] IEEE Std 802.3-2015: Subclause 33.4.9.1.2—,Equation 33-19.
[2] IEEE Std 802.3-2015: Subclause 33.9.3.5, Item PSEEL11
[3] UNH-IOL Clause 33 PSE Parametric Test Suite Test # 33.4.2

This test is no longer required.

GROUP 5: PSE DATA LINK LAYER CLASSIFICATION

Scope: The following tests cover data link layer classification tests specific to Type 1 and Type 2 Power Sourcing Equipment (PSEs).

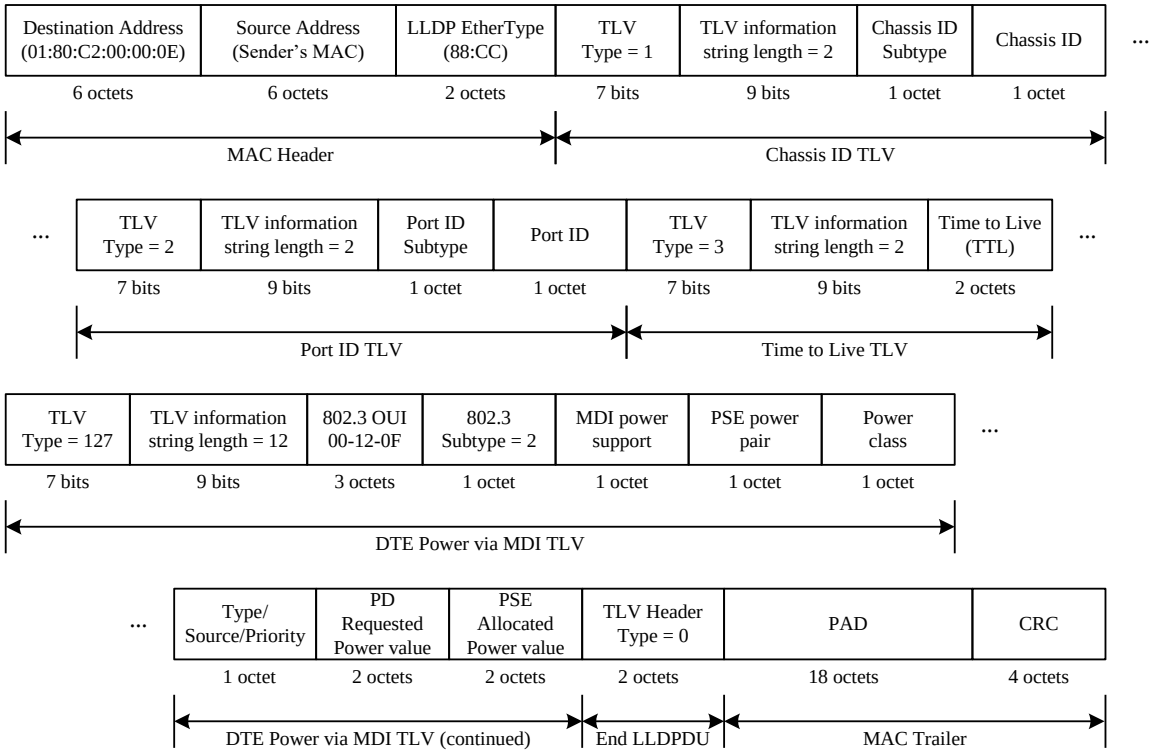
Overview: These tests apply to IEEE Std 802.3-2015 Clause 33 PoE devices. Specifically, the problems related to the function of Data Link Layer Classification.

PSE.5.26: TLV Frame Definition

Purpose: To verify that DTE Power via MDI TLV frames are properly formatted.

Reference:
[1] IEEE Std 802.3-2015 Subclause 33.6.1
[2] IEEE Std 802.3-2015 Subclause 79.3.2
[3] IEEE Std 802.1AB-20XX
[4] IEEE Std 802.1AB-2005
[5] UNH-IOL Clause 33 PSE Data Link Layer Classification Test Suite Test # 33.1.1

Discussion: A product that supports data link layer classification must meet the specified frame definition in order to ensure interoperability. The DTE Power via MDI TLV is contained within an LLDPDU. The LLDPDU has three mandatory TLVs followed by the DTE Power via MDI TLV. Within the DTE Power via MDI TLV there are several defined fields within the TLV header and TLV information string. Each of these fields must be properly formatted to included length and proper bit maps so they may be properly interpreted.



DTE Power via MDI TLV Format

Test Setup: Connect the DUT to the Testing equipment with a short cable (approximately 1m in length).

Procedure:
1. Capture a LLDPDU DTE Power via MDI TLV exchange.
2. Verify that the DTE Power via MDI TLV frame is properly formatted.

Observable Results:
The fields of the LLDPDU DTE Power via MDI TLV should be as follows:

MAC Header		
Destination Address	01:80:C2:00:00:0E	The Destination Address field specifies the station(s) for which the frame is intended, in this case the LLDP multicast address
Source Address	XX:XX:XX:XX:XX:XX	The Source Address field specifies the station sending the frame.
LLDP EtherType	88:CC	The Length/Type field indicates the nature of the MAC client protocol, in this case the LLDP Ethertype.
Chassis ID TLV		
Chassis ID TLV	**TLV type** Type = 1 **TLV information string length** Length = 2 (octets) **Chassis ID subtype** 0 = Reserved 1 = Chassis component 2 = Interface alias 3 = Port component 4 = MAC address 5 = Network address 6 = Interface name 7 = Locally assigned 8 – 255 = Reserved **Chassis ID** 1 to 255 octets	The Chassis ID TLV is a mandatory TLV that identifies the chassis containing the IEEE 802 LAN station associated with the transmitting LLDP agent. The Chassis ID TLV shall be the first TLV in the LLDPDU. The TLV information string length field shall indicate the exact length, in octets. The chassis ID subtype field shall contain an integer value indicating the basis for the chassis ID entity that is listed in the chassis ID field. The chassis ID field shall contain an octet string indicating the specific identifier for the particular chassis in this system. An LLDPDU shall contain exactly one Chassis ID TLV.
Port ID TLV		
Port ID TLV	**TLV type** Type = 2 **TLV information string length** Length = 2 (octets) **Port ID subtype** 0 = Reserved 1 = Interface alias 2 = Port component 3 = MAC address 4 = Network address 5 = Interface name 6 = Agent circuit ID 7 = Locally assigned 8 – 255 = Reserved **Port ID** 1 to 255 octets	The Port ID TLV is a mandatory TLV that identifies the port component of the MSAP identifier associated with the transmitting LLDP agent. The Port ID TLV shall be the second TLV in the LLDPDU. The TLV information string length field shall indicate the length, in octets. The port ID subtype field shall contain an integer value indicating the basis for the identifier that is listed in the port ID field. The port ID field is an alpha-numeric string that contains the specific identifier for the port from which this LLDPDU was transmitted. An LLDPDU shall contain exactly one Port ID TLV.

Time to Live TLV		
Time to Live TLV	**TLV type** Type = 3 **TLV information string length** Length = 2 (octets) **Time to Live (TTL)** An integer value in the range $0 \leq t \leq 65535$ in seconds	The Time To Live TLV indicates the number of seconds that the recipient LLDP agent is to regard the information associated with this MSAP identifier to be valid. The Time To Live TLV is mandatory and shall be the third TLV in the LLDPDU. The TTL field shall contain an integer value in the range $0 \leq t \leq 65535$ seconds and shall be set to the computed value of txTTL at the time the LLDPDU is constructed. An LLDPDU shall contain exactly one Time To Live TLV.
DTE Power via MDI TLV		
TLV type & Information String Length	**TLV Type** Type = 127 **TLV information string length** Length = 12 (octets)	An LLDPDU should contain no more than one Power Via MDI TLV.
802.3 OUI	00:12:0F	3-octet organizationally unique identifier.
802.3 subtype	02	1-octet organizationally defined subtype.
MDI power support	**Reserved: Bits 7:4** **PSE Pair Control Ability Supported: Bit 3** 0 = Not supported 1 = Supported **PSE MDI Power State Enabled: Bit 2** 0 = Disabled 1 = Enabled **PSE MDI Power Support: Bit 1** 0 = Not supported 1 = Supported **Port Class: Bit 0** 0 = PD 1 = PSE	The MDI power support field shall contain a bit-map of the MDI power capabilities and status.
PSE power pair	Alternative A = 01 Alternative B = 02	The PSE power pair field shall contain an integer value as defined by the pethPsePortPowerPairs object in IETF RFC 3621.
Power class	Class 0 = 01 Class 1 = 02 Class 2 = 03 Class 3 = 04 Class 4 = 05	The power class field shall contain an integer value as defined by the pethPsePortPowerClassifications object in IETF RFC 3621.
Type/source/priority	**Power type: Bits 7:6** 11 = Type 1 PD 10 = Type 1 PSE	The power type/source/priority field shall contain a bit-map of the power type, source and priority.

	01 = Type 2 PD 00 = Type 2 PSE **Power source: Bits 5:4** ***Where power type = PD*** 11 = PSE and local 10 = Local 01 = PSE 00 = Unknown ***Where power type = PSE*** 11 = Reserved 10 = Backup source 01 = Primary power source 00 = Unknown **Reserved: Bits 3:2** **Power Priority: Bits 1:0** 11 = Low 10 = High 01 = Critical 00 = Unknown (default)	
PD requested power value	Power = 0.1 × (decimal value of bits) Watts.	Valid values for these bits are decimal 1 through 255.
PSE allocated power value	Power = 0.1 × (decimal value of bits) Watts.	Valid values for these bits are decimal 1 through 255.
End of LLDPDU TLV		
End of LLDPDU TLV	**TLV Type** Type = 0	A 2 octet, all-zero TLV used to mark the end of the TLV sequence in LLDPDUs.
MAC Trailer		
MAC Pad	All zeros	If necessary, the data field is extended by appending extra bits (that is, a pad) in units of octets after the data field but prior to calculating and appending the FCS.
CRC	32 bit Frame Check Sequence	A cyclic redundancy check (CRC) is used by the transmit and receive algorithms to generate a CRC value for the FCS field.

Possible Problem: None

PSE.5.27: Data Link Layer Classification Timing Requirements

Purpose: To verify that DTE Power via MDI TLV frames are transmitted within the proper timing constraints.

Reference:
[1] IEEE Std 802.3-2015 Subclauses 33.2.4.4, 33.6.2 and 33.6.3.3
[2] UNH-IOL Clause 33 PSE Data Link Layer Classification Test Suite Test # 33.1.2

Discussion: A Type 1 PSE that implements Data Link Layer classification shall send an LLDPDU containing a Power via MDI TLV when the PSE Data Link Layer classification engine is ready as indicated by the variable pse_dll_ready (33.6.3.3).

A Type 2 PSE shall send an LLDPDU containing a Power via MDI TLV within 10 seconds of Data Link Layer classification being enabled in the PSE as indicated by the variable pse_dll_enabled (33.2.4.4, 33.6.3.3).

Test Setup: Connect the DUT to the Testing equipment with a short cable (approximately 1m in length).

Procedure:
1. Power off the PSE or disable Data Link Layer Classification.
2. Power on the PSE and/or enable Data Link layer Classification.
3. Capture the transmission from the PSE.

Observable Results:
The PSE should transmit a valid Power via MDI TLV.
A Type 2 PSE should transmit the TLV within 10 seconds of the Data Link Layer classification being enabled as indicated by pse_dll_enabled.

Possible Problem: None

PSE.5.28: "PD requested power value" field changed

Purpose: To verify that a PSE transmits an updated LLDPDU within 10 seconds upon receipt of an updated "PD requested power value".

Reference:
[1] IEEE Std 802.3-2015 Subclause 33.6.2
[2] IEEE Std 802.3-2015 Figure 33–27
[3] UNH-IOL Clause 33 PSE Data Link Layer Classification Test Suite Test # 33.1.3

Discussion: Under normal operation, an LLDPDU containing a Power via MDI TLV with an updated value for the "PSE allocated power value" field shall be sent within 10 seconds of receipt of an LLDPDU containing a Power via MDI TLV where the "PD requested power value" field is different from the previously communicated value.

Test Setup: Connect the DUT to the Testing equipment with a short cable (approximately 1m in length).

Procedure:
1. Instruct the Testing equipment to transmit a Power via MDI TLV with a PD requested power value different than the previously communicated value.
2. Capture the resulting LLDPDU exchange.

Observable Results:
The DUT should transmit a valid Power via MDI TLV with an updated PSE allocated power value within 10 seconds upon receipt of the TLV from the Test Equipment.

Possible Problem: None.

PSE.5.29: PSE in Sync with PD

Purpose: To verify that the PSE increases its power allocation only when it is in sync with the PD.

Reference:
[1] IEEE Std 802.3-2015 Subclause 33.6.4.1
[2] IEEE Std 802.3-2015 Figure 33–27
[3] UNH-IOL Clause 33 PSE Data Link Layer Classification Test Suite Test # 33.1.4

Discussion: A PSE is considered to be in sync with the PD when the value of PSEAllocatedPowerValue matches the value of MirroredPSEAllocatedPowerValueEcho. When the PSE is not in sync with the PD, the PSE is only allowed to decrease its power allocation.

Test Setup: Connect the DUT to the Testing equipment with a short cable (approximately 1m in length).

Procedure:
1. Instruct the Testing equipment to transmit a Power via MDI TLV with a PSE allocated power value different than the previously communicated value.
2. Capture the resulting LLDPDU exchange.
3. Repeat steps 1 and 2 with varying values for the PSE allocated power value.

Observable Results:
The DUT should only increase its power allocation when in sync with the PD.

Possible Problem: None.

PD Tests

GROUP 1: PD ELECTRICAL CHARACTERISTICS

Scope: The following tests cover parametric tests specific to Type 1 and Type 2 Powered Products (PDs).

Overview:
These tests apply to IEEE Std 802.3-2015 Clause 33 PoE devices. Specifically, the problems related to the functional and electrical characteristics of Powered Devices.

PD.1.1: Source Power

Purpose: To verify that DUT does not source power on its power interface (PI).

Reference:
[1] IEEE Std 802.3-2015: Subclause 33.3.1, Table 33-13, Item PD3
[2] UNH-IOL Clause 33 PD Parametric Test Suite Test # 33.1.1

Discussion: A PD should not be capable of sourcing power on either of the two sets of PI conductors at any time.

Test Setup: Connect the Mode A positive V_{port} pins of the DUT to the positive terminal of the voltmeter, and the negative V_{port} pins to the negative terminal of the voltmeter. If the DUT has an alternate, non-PoE power source, use it to power the DUT.

Procedure:
1. Measure V_{Port} at the PI of the DUT using a voltmeter.
2. Verify that there is no power present at the PI.
3. Repeat steps 1 and 2 for Mode B.

Observable Results:
The DUT should not source power onto the PI at any time.

Possible Problem: None

PD.1.2: Valid PD Pinout

Purpose: To verify that the DUT is insensitive to the polarity of the power supply and is able to operate in either Mode A or Mode B.

Reference:
[1] IEEE Std 802.3-2015: Subclause 33.3.1, Table 33-13
[2] UNH-IOL Clause 33 PD Parametric Test Suite Test # 33.1.2

Discussion: After detection and optional classification, a PSE may supply power on either set of the four wire pairs, hence the PD must support drawing its power from both Mode A and Mode B regardless of the polarity of the power supply.

Table 33–13—PD pinout

Conductor	Mode A	Mode B
1	Positive V_{Port_PD}, Negative V_{Port_PD}	
2	Positive V_{Port_PD}, Negative V_{Port_PD}	
3	Negative V_{Port_PD}, Positive V_{Port_PD}	
4		Positive V_{Port_PD}, Negative V_{Port_PD}
5		Positive V_{Port_PD}, Negative V_{Port_PD}
6	Negative V_{Port_PD}, Positive V_{Port_PD}	
7		Negative V_{Port_PD}, Positive V_{Port_PD}
8		Negative V_{Port_PD}, Positive V_{Port_PD}

Test Setup: Connect the Mode A positive V_{port} pins of the DUT to the positive terminal of the power supply, and the negative V_{port} pins to the negative terminal of the power supply.

Procedure:
1. Apply power to the PI using Alternative A MDI.
2. Observe the operational status of the DUT.
3. Repeat steps 1 and 2, however, applying power on Mode A MDI-X, Mode B MDI, and Mode B MDI-X.

Observable Results:
In all cases the DUT should accept the applied power and become operational once the requested power has been supplied.

Possible Problem: None

PD.1.3: Valid Detection Signature Characteristics

Purpose: To verify that the DUT presents a valid detection signature while it is requesting power on the power interface (PI).

References:
[1] IEEE Std 802.3-2015: Section 33.3.4, Table 33-14, Figure 33-17
[2] UNH-IOL Clause 33 PD Parametric Test Suite Test # 33.1.3

Discussion: If a PD will accept power, but is not powered, via the PI then it should present a valid detection signature at the PI between the positive and negative V_{Port} pins for both pinout Modes such that the attached PSE will properly detect the PD's request for power. The standard defines the signature to be comprised of five characteristics: a valid resistance, capacitance, and inductance; and either a voltage offset or a current offset. The voltage offset limit was specified to allow for the inherent voltage offset for two series diode drops. Similarly, the current limit allows for internal FET leakage. Given the minimum and maximum limits on the defined resistive slope, there are no minimum bounds for the offset components as a maximum current implies a minimum voltage, and vice versa. Figure 33-17, reproduced below, illustrates the signature resistance and voltage offsets.

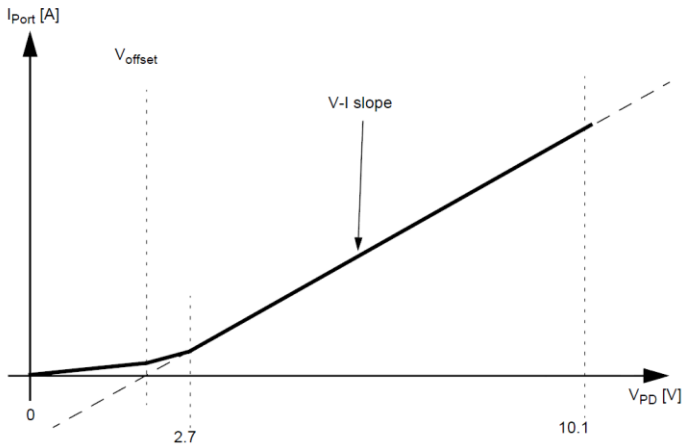


Figure 33–17—Valid PD detection signature offset

Test Setup: Connect the Mode A positive V_{port} pins of the DUT to the positive terminal of the power supply, and the negative V_{port} pins to the negative terminal of the power supply.

Procedure:

1. Limit the power supply current between 4 to 5 mA.
2. Applying voltage using Alternative A, vary the power supply voltage, V_N, with at least two values from 0.0 V to 10.2and measure the corresponding current, I_N, drawn by the DUT.
3. Calculate R_{sigN} using a 1 V chord between measurement points.
4. Determine either the voltage offset or the current offset by calculating the intersection of the line between the (V_N, I_N) and (V_{N+1}, I_{N+1}) data points and V/I axis.
5. Repeat steps 1-4 for any additional values that the test and measurement equipment supports.
6. Repeat steps 1-5, however, connect the DUT to accept power on Mode B.

Observable Results:
In step 4 the observed signature resistance should be between 23.75 KΩ and 26.3KΩ (inclusive).

In step 5 the DUT should have either a voltage offset less than or equal to 1.9 V, or a current offset less than 12 μA.

Possible Problems: None

PD.1.4: Non-Valid Detection Signature Characteristics

Purpose: To verify that the DUT presents a non-valid detection signature while it is not requesting power, or once powered, at the power interface (PI) of the non-powered pairs.

Reference:
[1] IEEE Std 802.3-2015: Subclause 33.3.4, Table 33-15
[2] UNH-IOL Clause 33 PD Parametric Test Suite Test # 33.1.4

Discussion: There are two cases when a PD should present a non-valid detection signature when attached to the PSE via the PI. The first case is while a PD is in a state where it will not accept power via the PI. The second case occurs once a PD becomes powered via the PI, and it must present a non-valid detection signature on the set of pairs from which it is not drawing power.

Test Setup: Connect the Mode A positive V_{port} pins of the DUT to the positive terminal of the power supply, and the negative V_{port} pins to the negative terminal of the power supply.

Procedure:
1. Limit the power supply current between 4 to 5 mA.
2. Applying voltage using Alternative A, and confirm the DUT is drawing power via the PI.
3. Applying voltage to the non-powered pairs, vary the power supply voltage with at least two values, Vn, from 0.0 V to 10.2V and measure the corresponding current, IN, drawn by the DUT.
4. Calculate RsigN using a 1 V chord between measurement points.
5. Repeat steps 1-4 for any additional values that the test and measurement equipment support.

Repeat steps 1-5, however, connect the DUT to accept power on Mode B.

Observable Results:
In step 5 verify that $Rsig_N < 12\ K\Omega$ or $Rsig_N > 45\ K\Omega$.

Possible Problems: None

PD.1.5: Input Average Power

Purpose: To verify that the PD does not draw more power than allowed for each class.
Reference:
[1] IEEE Std 802.3-2015: Subclause 33.3.7.2, Table 33-18
[2] UNH-IOL Clause 33 PD Parametric Test Suite Test # 33.1.5

Discussion: For a PD that supports classification, the maximum power that the PD may draw across all input voltages and operational modes is governed by the limits specified in table 33-18. This value is known as P_{CLASS}_PD.

Derived From Item 4 of Table 33-18

Class	Maximum power available to PD	PD Type
0	13.0 Watts	1
1	3.84 Watts	1
2	6.49 Watts	1
3	13.0 Watts	1
4	25.5 Watts	2

Test Setup: Connect the Mode A positive V_{port} pins of the DUT to the positive terminal of the power supply, and the negative V_{port} pins to the negative terminal of the power supply.

Procedure:

1. 1. Apply a port voltage of 37 V for Class 1-3 PDs, and 42.5 V for Class 4 PDs, onto the PI using Alternative A. Measure the current drawn by the DUT and calculate the input power averaged over a 1 second period for at least 5 minutes.
2. 2. Apply a port voltage of 57 V onto the PI using Alternative A. Measure the current drawn by the DUT and calculate the input power averaged over a 1 second period for at least 5 minutes.
3. Repeat steps 1-2, however, apply power using Alternative B.

Observable Results:
The maximum power drawn by the DUT for each supported class should be below the maximum value specified in table 33-18.

Possible Problems: It may be difficult to get a PD to draw its maximum power depending on the products deisgned purpose.

PD.1.6: PD Input Voltage

Purpose: To verify that the DUT will turn on once power has been applied to the power interface (PI), will remain on over the entire port voltage range, and turn off once power is removed.

Reference:
[1] IEEE Std 802.3-2015: Subclause 33.3.7.1, Table 33-18
[2] UNH-IOL Clause 33 PD Parametric Test Suite Test # 33.1.7

Discussion: After startup, a PD is required to turn on its power supply before the input voltage (V_{port}) level reaches 42 V. Once turned on, the power supply then must remain on over the entire range of V_{port}, which is specified from 37 V to 57 V for a Type 1 PD and 42.5V to 57V for a Type 2 PD, as the attached PSE may vary the applied voltage on the PI over this range at any time. If the minimum value of V_{port} is not maintained by the PSE, the PD must turn off before the input voltage level reaches 30 V.

Test Setup: Connect the Mode A positive V_{port} pins of the DUT to the positive terminal of the power supply, and the negative V_{port} pins to the negative terminal of the power supply.

Procedure:
1. Apply 42 V across the PI.
2. Observe the operational status of the DUT.
3. Repeat steps 1 and 2, however, increment the applied voltage until the DUT has become fully operational.
4. Once operational, increase the applied voltage to 57 V in any increment supported by the Test Equipment, and then decrease the voltage to 49 V.
5. Observe the operational status of the DUT.
6. Decrease the applied voltage by in any increment supported by the Test Equipment.
7. Observe the status of the DUT.
8. Repeat steps 6 and 7 until the DUT turns off.

Repeat steps 1-8, however, connect the DUT to accept power on Mode B.

Observable Results:
The DUT should become fully operational at a port voltage less than 42 V.
Once the DUT has turned on, it should remain operational for V_{PORT} between 37 V and 57 V for a Type 1 PD and 42.5V to 57V for a Type 2 PD.
The DUT should turn off at a port voltage greater than 30V and less than 37 V for a Type 1 PD. A Type 2 PD should turn off at a port voltage greater than 30V and less than 41 V.

Possible Problems: None

PD.1.7: PD Maintain Power Signature

Purpose: To verify that DUT provides a valid Maintain Power Signature (MPS) at the PI.

Reference:
[1] IEEE Std 802.3-2015: Subclause 33.3.8, Table 33-19
[2] UNH-IOL Clause 33 PD Parametric Test Suite Test # 33.1.8

Discussion: A PD must provide a valid Maintain Power Signature (MPS) so that a PSE will remain powering the PD. The MPS must be valid for both DC and AC components. The DUT must provide valid DCMPS, which is a current draw equal to or above I_{port} for a minimum duration of 75ms followed by an optional dropout for a maximum of 250ms. The DUT must also provide a valid ACMPS, which requires the DUT to have a maximum input resistance of R_{pd_d} and a minimum input capacitance of C_{pd_d}. These values are outlined in Table 33-19.

Table 33–19—PD Maintain Power Signature

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Input current	I_{Port_MPS}	A	0.010		See 33.3.8
2	Input resistance	R_{pd_d}	kΩ		26.3	
3	Input capacitance	C_{pd_d}	µF	0.050		See Table 33–12

Test Setup: Connect the Mode A positive V_{port} pins of the DUT to the positive terminal of the power supply, and the negative V_{port} pins to the negative terminal of the power supply. Monitor voltage and current.

Procedure:
1. Apply 44 Volts to the PI.
2. Measure the current draw.
3. Repeat steps 1 and 2 for voltages in the range of 44-57 Volts supported by the Test Equipment.
4. Calculate the input resistance from the measurements obtained in steps 1-3.
5. Repeat steps 1-4; however, connect the DUT to accept power on Mode B.

Observable Results:
The current draw is greater than or equal to 10mA (I_{port}) for at least 75 ms over the range of 44-57 Volts.
A current draw of less than 10mA should not last more than 250 ms over the range of 44-57 Volts.
The input resistance is less than or equal to 26.3kΩ (R_{pd_d}) over the range 44-57 Volts.

Possible Problems: None

PD.1.8: PD Input Inrush Current Timing (Informative)

Purpose: To verify that the PD input inrush current timing is within conformant limits.

Reference:
[1] IEEE Std 802.3-2015: Subclause 33.3.7.3, Table 33-11
[2] UNH-IOL Clause 33 PD Parametric Test Suite Test # 33.1.9

Discussion: This test measures the length of time the PD's input inrush current exists. It is defined as the time from the application of V_{PORT} to the time when C_{PORT} is charged to 99% of its final value.

Test Setup: Using the Test Equipment, connect the Mode A positive V_{port} pins of the DUT to the positive terminal of the power supply, and the negative V_{port} pins to the negative terminal of the power supply.

Procedure:
1. Apply a port voltage of 44 V onto the PI using Alternative A.
2. Using an oscilloscope, measure $T_{INRUSH.}$
3. Repeat steps 1-2, however, apply power using Alternative B.
4. Repeat steps 1-3 with a port voltage of 57 V.

Observable Results:
In step 2 and 3, the current is less than 400mA at the 50ms mark after power is applied

Possible Problems: None

PD.1.9: Peak Transient Current

Purpose: To verify that the PD peak current transients and levels are within conformant limits.

Reference:
[1] IEEE Std 802.3-2015: Subclause 33.3.7.5, Figure 33-18, Table 33-18
[2] UNH-IOL Clause 33 PD Parametric Test Suite Test # 33.1.10

Discussion: With a static input voltage at the PI, after inrush, the PD should limit the transient current draw. The transients should not exceed 4.7mA/µs for either polarity. These transients should not exceed P_{Peak_PD} and also must not exceed P_{Class_PD} for longer than T_{cut}min per figure 33-18.

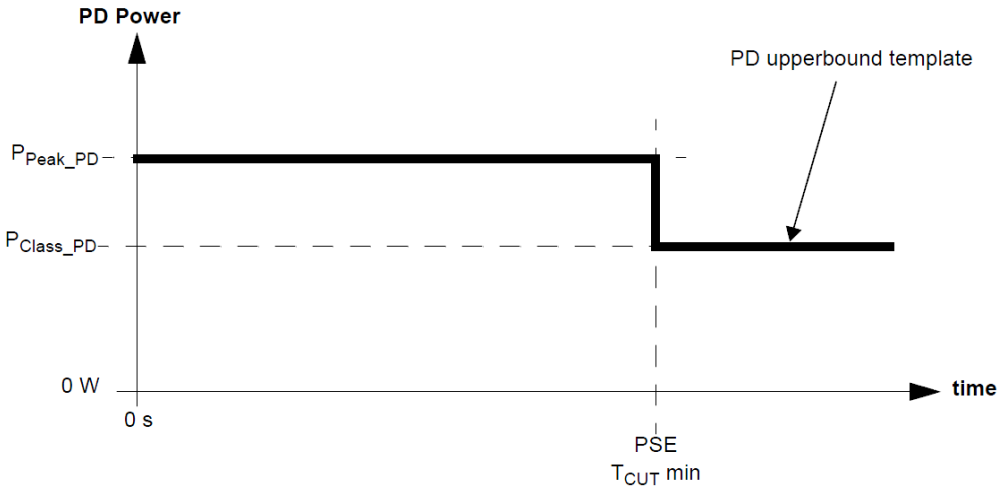


Figure 33–18—PD static operating mask

Test Setup: Using the Test Equipment, connect the Mode A positive V_{port} pins of the DUT to the positive terminal of the power supply, and the negative V_{port} pins to the negative terminal of the power supply. Monitor the current draw with the current probe.

Procedure:
1. Apply a valid static input voltage at the PI of the PD.
2. Attempt to get the PD to rapidly change its current draw.

Monitor the current draw for at least a 5 minute period.

Observable Results:
During the monitoring period the current draw should be less than the PD static operating mask as defined in Figure 33-18.

Possible Problems: It may be difficult to get a PD to rapidly change current draw, especially for consumer end products.

GROUP 2: PD CLASSIFICATION TESTS

Scope: The following tests cover classification tests specific to Type 1 and Type 2 Powered Products (PDs).

Overview: These tests apply to IEEE Std 802.3-2015 Clause 33 PoE devices. Specifically, the problems related to the functional and electrical characteristics of classification for Powered Devices.

PD.2.10: Allowed Classification Permutations

Purpose: To verify whether the PD fits a valid classification permutation.

References:
[1] IEEE Std 802.3-2015: Subclause 33.2.8, Table 33–8
[2] UNH-IOL Clause 33 PD Parametric Test Suite Test # 33.2.1

Discussion: A PD shall meet one of the allowable classification permutations listed in Table 33–8.

A Type-2 PD shall meet at least one of the allowable classification permutations listed in Table 33-8. If a Type-2 PD does not successfully observe a 2-Event Physical Layer classification or Data Link Layer classification, the PD must conform to Type-1 power restrictions.

Permutations			PSE allowed?	PD allowed?
PSE/PD Type	Physical Layer classification	Data Link Layer classification		
Type 2	2-Event	No	Yes	No
		Yes	Yes	Yes
	1-Event	No	No	No
		Yes	Yes	No
	None	No	No	No
		Yes	No	No
Type 1	2-Event	No	No	Yes
		Yes	No	Yes
	1-Event	No	Yes	Yes
		Yes	Yes	Yes
	None	No	Yes	No
		Yes	Yes	No

Table 33-8

Test Setup: The DUT is connected to the Test Equipment with a short cable (approximately 1m in length).

Procedure for Type 1 PD:
1. Use the Test equipment to perform a 1-event classification and power the DUT.
2. Determine the DUTs Class Current Draw.
3. Monitor for Data Link Layer classification for more than 5 minutes.
4. Repeat steps 1-3 with a 2-event classification.

Procedure for Type 2 PD:
1. Configure the Test Equipment to perform a 1-Event physical layer classification after detection has been completed transmit a Power via MDI TLV with the PSE allocated power field equivalent set to 26.20 watts and observe results.
2. Configure the Test Equipment to perform a 2-Event physical layer classification after detection has been completed transmit a Power via MDI TLV with the PSE allocated power field equivalent set to 26.20 watts and observe results.
3. Configure the Test Equipment to perform a 1-Event physical layer classification after detection has been completed do not complete a data link layer classification and observe results.

Observable Results:
AType 1DUT should meet an allowable permutation as shown in table 33-8
In steps 1 and 2 a Type 2 DUT should accept power, become operational, and perform a data link layer classification.
In step 3 a Type 2 DUT that does not conform to Type 1 PD power restriction must provide an active indication that it is underpowered.

Possible Problems: None.

PD.2.11: Single Event Physical Layer Classification

Purpose: To verify that a PD returns the correct classification current draw.

Reference:
[1] IEEE Std 802.3-2015: Subclause 33.3.5.1, Table 33-16
[2] UNH-IOL Clause 33 PD Parametric Test Suite Test # 33.2.2

Discussion: The purpose of PD classification is to provide the PSE information about the maximum power that the PD will draw across all input voltages and operational modes. A PD should present one and only one classification signature during classification. By default, a type 1 PD is Class 0; however, to improve power management for the PSE, a PD may provide a signature for Class 1 to 3, which are outlined in table 33-16. Type 2 PDs implementing 1 event classification shall respond with a Class 4 signature.

Table 33-16 - Classification signature, measured at PD input connector

Parameter	Conditions	Minimum	Maximum	Unit
Current for Class 0	14.5 V to 20.5 V	0	4.00	mA
Current for Class 1	14.5 V to 20.5 V	9.00	12.0	mA
Current for Class 2	14.5 V to 20.5 V	17.0	20.0	mA
Current for Class 3	14.5 V to 20.5 V	26.0	30.0	mA
Current for Class 4	14.5 V to 20.5 V	36.0	44.0	mA

Test Setup: Connect the Mode A positive V_{port} pins of the DUT to the positive terminal of the power supply, and the negative V_{port} pins to the negative terminal of the power supply.

Procedure:
1. Apply power onto the PI using Alternative A, with a voltage from 14.5V to 20.5V.
2. Measure the corresponding current drawn by the DUT.
3. Repeat steps 1-2 for any voltage increments supported by the Test Equipment.
4. Repeat steps 1-3, however, connect the DUT to accept power on Mode B.

Observable Results:
In step 2 the current drawn by the DUT for each supported class should be within the range (inclusive) specified in table 33-16.
The DUT should only present one classification signature during classification.

Possible Problems: None.

PD.2.12: Two Event Physical Layer Classification

Purpose: To verify that a Type-2 PD correctly implements two-event physical layer classification.

Reference:
[1] IEEE Std 802.3-2015: Subclause 33.3.5.2, Table 33-15, Table 33-17, Table 33-18, Figure 33-16
[2] UNH-IOL Clause 33 PD Parametric Test Suite Test # 33.2.3

Discussion: A Type-2 PD's behavior must conform to the state diagram defined in Figure 33-16 The PD must present valid current draws at all states within the state diagram. The PD shall return a Class 4 classification signature in accordance with the maximum power draw, P_{Class_PD}, as well as conform to electrical requirements as specified by Table 33–18. This test applies the appropriate voltages and checks DUT behavior to determine whether or not the DUT steps through the state diagram correctly.

Test Setup: Attach the PI of the DUT to the class pulse test equipment. Monitor PI voltage and current with the DSO.

Procedure:

1. Apply power consistent with detection timing and amplitude to the PI on Mode A.
2. Apply a 2-event classification pulse with timing and amplitude that are close to the minimum timing and minimum amplitude parameters.
3. Measure current for all stages of 2-event classification.
4. Apply power to the PI on Mode A.
5. Check for external indication that a 2-event class pulse was received.
6. Repeat steps 1-5 for different combinations of timing and amplitude that are close to the minimum and maximum timing and amplitude parameters.
7. Repeat steps 1-6 for Mode B.
8. Measure V_{RESET} by repeating steps 1-5 and setting V_{MARK2} to a voltage below 2.8 volts and increasing it until the product exhibits a 2 event response.
9. Repeat steps 1-5, but in step two apply a voltage at or slightly below the V_{RESET} value measured in step 8 for V_{MARK1}.

Observable Results:
The DUT should successfully transition throughout the state diagram.
In step 5 for conformant 2-event pulses, the DUT should indicate that a 2-event class pulse was received, either through external indication or through a power draw exceeding the maximum Type 1 power in step 4 (not to exceed the maximum Type 2 power draw).
In step 3, classification current draw for both pulses should be within 36 and 44mA for a Type 2 PD. For a Type 1 PD this shall indicate a valid current draw based on the PD's Class (0-3) for both pulses.
In step 3, I_{Mark} should be within 0.25-4.00mA.
In step 3, the DUT should present an invalid detection signature during V_{MARK1} and $V_{MARK2.}$ Unless the input capacitance is greater than 10uF, the maximum resistance detected should be 12KΩ when V_{MARK1} and V_{MARK2} are varied between 6.9V and 10.1V.
In step 8, determine whether the application of V_{RESET} successfully restarts the classification process. If external indication of 2-event class pulse is available, the DUT should not indicate that it has received a 2-event class pulse after $V_{RESET.}$ Check the maximum power draw to ensure that the PD does not exceed maximum power for a Type 1 product.

Possible Problems: This test is not applicable to Type 1 PDs that do not implement 2-event physical layer classification.

PD.2.13: Classification Stability Time

Purpose: To verify that classification current draw of the DUT is valid within T_{class}.

Reference:
[1] IEEE Std 802.3-2015: Subclause 33.3.7.8, Table 33-16, Table 33-17, Table 33-18
[2] UNH-IOL Clause 33 PD Parametric Test Suite Test # 33.2.4

Discussion: When the PSE performs a class event, the PI of a PD is probed with a voltage in the range of 14.5V to 20.5V. The classification level of the PD is determined by observing the current draw. The classification current draw of the PD must be valid before 5ms (T_{class}), so that the PSE will properly detect the PD. The classification currents are outlined in Table 33-16.

Test Setup:. Attach the PI of the DUT to the class pulse test equipment. Monitor PI voltage and current with the DSO.

Procedure:
1. Apply a class pulse at the minimum condition of 14.5 Volts.
2. Measure the delay between the rising edge of the class pulse and the point when the valid classification current level is reached.
3. Observe the current draw after T_{class}.
4. Repeat steps 1-3 with the maximum condition of 20.5 Volts.
5. Repeat steps 1-4; however, connect the DUT to accept power on Mode B.

Observable Results:
The classification current draw is valid within 5ms (T_{class}).
The classification current draw is within the valid range for all times after T_{class}.

Possible Problems: None.

GROUP 3: PD DATA LINK LAYER CLASSIFICATION

Scope: The following tests cover data link layer classification tests specific to Type 1 and Type 2 Powered Products (PDs). Note: This testing is not required for Type 2 PD Evaluation Platforms

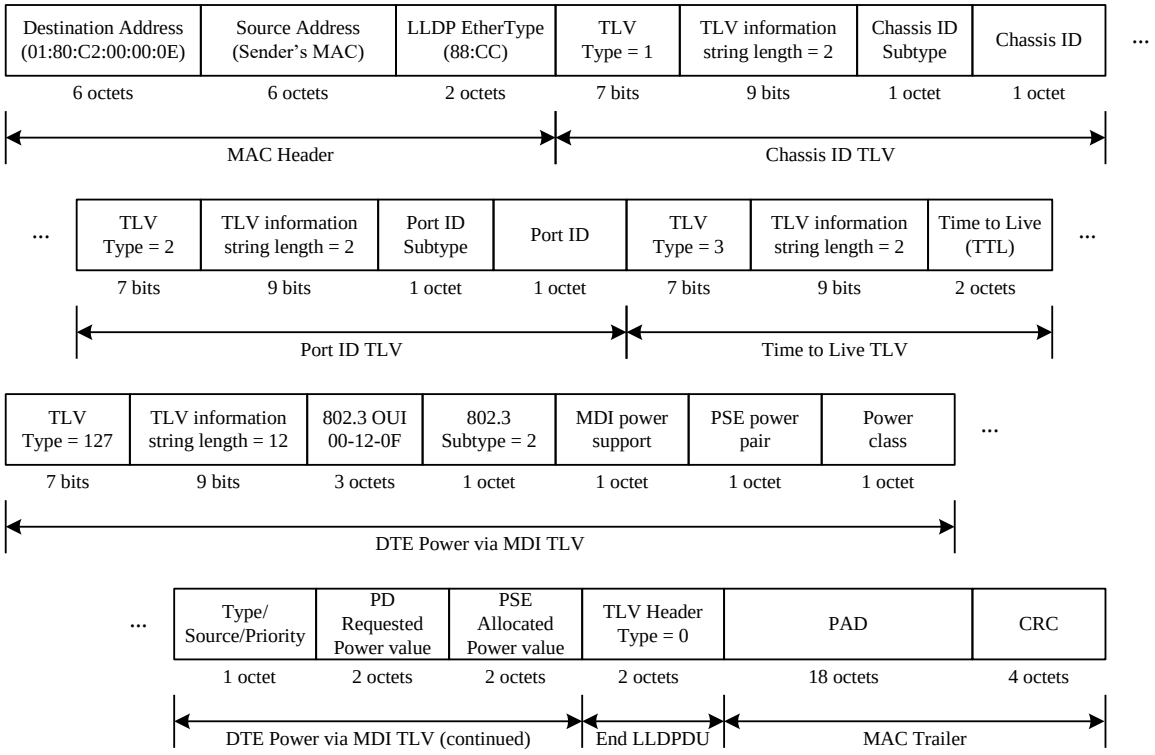
Overview: These tests apply to IEEE Std 802.3-2015 Clause 33 PoE devices. Specifically, the problems related to the function of Data Link Layer Classification for Powered Devices.

PD.3.14: TLV Frame Definition

Purpose: To verify that DTE Power via MDI TLV frames are properly formatted.

Reference:
[1] IEEE Std 802.3-2015 Subclause 33.6.1
[2] IEEE Std 802.3-2015 Subclause 79.3.2
[3] IEEE Std 802.1AB-20XX
[4] IEEE Std 802.1AB-2005
[5] UNH-IOL PD Data Link Layer Classification Test Suite Test # 33.1.1

Discussion: A product that supports data link layer classification must meet the specified frame definition in order to ensure interoperability. The DTE Power via MDI TLV is contained within an LLDPDU. The LLDPDU has three mandatory TLVs followed by the DTE Power via MDI TLV. Within the DTE Power via MDI TLV there are several defined fields within the TLV header and TLV information string. Each of these fields must be properly formatted to included length and proper bit maps so they may be properly interpreted.



DTE Power via MDI TLV Format

Test Setup: Connect the DUT to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
1. Capture a LLDPDU DTE Power via MDI TLV exchange between the DUT and the Test Equipment.
2. Verify that the DTE Power via MDI TLV frame is properly formatted.

Observable Results:
The fields of the LLDPDU DTE Power via MDI TLV should be as follows:

MAC Header		
Destination Address	01:80:C2:00:00:0E	The Destination Address field specifies the station(s) for which the frame is intended, in this case the LLDP multicast address
Source Address	XX:XX:XX:XX:XX:XX	The Source Address field specifies the station sending the frame.
LLDP EtherType	88:CC	The Length/Type field indicates the nature of the MAC client protocol, in this case the LLDP Ethertype.
Chassis ID TLV		
Chassis ID TLV	**TLV type** Type = 1 **TLV information string length** Length = 2 (octets) **Chassis ID subtype** 0 = Reserved 1 = Chassis component 2 = Interface alias 3 = Port component 4 = MAC address 5 = Network address 6 = Interface name 7 = Locally assigned 8 – 255 = Reserved **Chassis ID** 1 to 255 octets	The Chassis ID TLV is a mandatory TLV that identifies the chassis containing the IEEE 802 LAN station associated with the transmitting LLDP agent. The Chassis ID TLV shall be the first TLV in the LLDPDU. The TLV information string length field shall indicate the exact length, in octets. The chassis ID subtype field shall contain an integer value indicating the basis for the chassis ID entity that is listed in the chassis ID field. The chassis ID field shall contain an octet string indicating the specific identifier for the particular chassis in this system. An LLDPDU shall contain exactly one Chassis ID TLV.
Port ID TLV		
Port ID TLV	**TLV type** Type = 2 **TLV information string length** Length = 2 (octets) **Port ID subtype** 0 = Reserved 1 = Interface alias 2 = Port component 3 = MAC address 4 = Network address 5 = Interface name 6 = Agent circuit ID 7 = Locally assigned 8 – 255 = Reserved **Port ID** 1 to 255 octets	The Port ID TLV is a mandatory TLV that identifies the port component of the MSAP identifier associated with the transmitting LLDP agent. The Port ID TLV shall be the second TLV in the LLDPDU. The TLV information string length field shall indicate the length, in octets. The port ID subtype field shall contain an integer value indicating the basis for the identifier that is listed in the port ID field. The port ID field is an alpha-numeric string that contains the specific identifier for the port from which this LLDPDU was transmitted. An LLDPDU shall contain exactly one Port ID TLV.

Time to Live TLV		
Time to Live TLV	**TLV type** Type = 3 **TLV information string length** Length = 2 (octets) **Time to Live (TTL)** An integer value in the range $0 \leq t \leq 65535$ in seconds	The Time To Live TLV indicates the number of seconds that the recipient LLDP agent is to regard the information associated with this MSAP identifier to be valid. The Time To Live TLV is mandatory and shall be the third TLV in the LLDPDU. The TTL field shall contain an integer value in the range $0 \leq t \leq 65535$ seconds and shall be set to the computed value of txTTL at the time the LLDPDU is constructed. An LLDPDU shall contain exactly one Time To Live TLV.
DTE Power via MDI TLV		
TLV type & Information String Length	**TLV Type** Type = 127 **TLV information string length** Length = 12 (octets)	An LLDPDU should contain no more than one Power Via MDI TLV.
802.3 OUI	00:12:0F	3-octet organizationally unique identifier.
802.3 subtype	02	1-octet organizationally defined subtype.
MDI power support	**Reserved: Bits 7:4** **PSE Pair Control Ability Supported: Bit 3** 0 = Not supported 1 = Supported **PSE MDI Power State Enabled: Bit 2** 0 = Disabled 1 = Enabled **PSE MDI Power Support: Bit 1** 0 = Not supported 1 = Supported **Port Class: Bit 0** 0 = PD 1 = PSE	The MDI power support field shall contain a bit-map of the MDI power capabilities and status.
PSE power pair	Alternative A = 01 Alternative B = 02	The PSE power pair field shall contain an integer value as defined by the pethPsePortPowerPairs object in IETF RFC 3621.
Power class	Class 0 = 01 Class 1 = 02 Class 2 = 03 Class 3 = 04 Class 4 = 05	The power class field shall contain an integer value as defined by the pethPsePortPowerClassifications object in IETF RFC 3621.
Type/source/priority	**Power type: Bits 7:6** 11 = Type 1 PD 10 = Type 1 PSE	The power type/source/priority field shall contain a bit-map of the power type, source and priority.

	01 = Type 2 PD 00 = Type 2 PSE **Power source: Bits 5:4** ***Where power type = PD*** 11 = PSE and local 10 = Local 01 = PSE 00 = Unknown ***Where power type = PSE*** 11 = Reserved 10 = Backup source 01 = Primary power source 00 = Unknown **Reserved: Bits 3:2** **Power Priority: Bits 1:0** 11 = Low 10 = High 01 = Critical 00 = Unknown (default)	
PD requested power value	Power = 0.1 × (decimal value of bits) Watts.	Valid values for these bits are decimal 1 through 255.
PSE allocated power value	Power = 0.1 × (decimal value of bits) Watts.	Valid values for these bits are decimal 1 through 255.
End of LLDPDU TLV		
End of LLDPDU TLV	**TLV Type** Type = 0	A 2 octet, all-zero TLV used to mark the end of the TLV sequence in LLDPDUs.
MAC Trailer		
MAC Pad	All zeros	If necessary, the data field is extended by appending extra bits (that is, a pad) in units of octets after the data field but prior to calculating and appending the FCS.
CRC	32 bit Frame Check Sequence	A cyclic redundancy check (CRC) is used by the transmit and receive algorithms to generate a CRC value for the FCS field.

Possible Problem: None

PD.3.15: Set pd_dll_ready

Purpose: To verify that a PD sets pd_dll_ready variable within 5 minutes of Data Link Layer classification being enabled.

Reference:
[1] IEEE Std 802.3-2015 Subclause 33.6.2
[2] UNH-IOL PD Data Link Layer Classification Test Suite Test # 33.1.3

Discussion: All Type 1 PDs that implement Data Link Layer classification and Type 2 PDs shall set the state variable pd_dll_ready within 5 minutes of Data Link Layer classification being enabled in a PD as indicated by the variable pd_dll_enabled (33.3.3.3, 33.6.3.3).

Test Setup: Connect the DUT to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
1. Power on the DUT.
2. Monitor a data link layer classification exchange between the Test Equipment and the DUT within 5 minutes of powering the DUT.

Observable Results:
The DUT should participate in a data link layer classification exchange within 5 minutes of data link layer classification being enabled indicating that pd_dll_ready variable has been set.

Possible Problem: It may not be possible to observe the state of the pd_dll_ready variable directly.

PD.3.16: "PSE allocated power value" field changed

Purpose: To verify that a PD transmits an updated LLDPDU within 10 seconds upon receipt of an updated "PSE allocated power value".

Reference:
[1] IEEE Std 802.3-2015 Subclause 33.6.2
[2] IEEE Std 802.3-2015 Figure 33–28
[3] UNH-IOL PD Data Link Layer Classification Test Suite Test # 33.1.4

Discussion: Under normal operation, an LLDPDU containing a Power via MDI TLV with an updated value for the "PD requested power value" field shall be sent within 10 seconds of receipt of an LLDPDU containing a Power via MDI TLV where the "PSE allocated power value" field is different from the previously communicated value.

Test Setup: Connect the DUT to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
1. Instruct the Test equipment to transmit a Power via MDI TLV with a PSE allocated power value different than the previously communicated value.
2. Capture the resulting LLDPDU exchange.

Observable Results:
The DUT should transmit a Power via MDI TLV with an updated PD requested power value within 10 seconds upon receipt of the TLV from the Test Equipment.

Possible Problem: None.

PD.3.17: PD in Sync with PSE

Purpose: To verify that the PD changes its maximum power draw or requested power only when it is in sync with the PSE.

Reference:
[1] IEEE Std 802.3-2015 Subclause 33.6.4.2
[2] IEEE Std 802.3-2015 Figure 33–28
[3] UNH-IOL PD Data Link Layer Classification Test Suite Test # 33.1.5

Discussion: A PD is considered to be in sync with the PSE when the value of PDRequestedPowerValue matches the value of MirroredPDRequestedPowerValueEcho. The PD is not allowed to change its maximum power draw or the requested power value when it is not in sync with the PSE.

Test Setup: Connect the DUT to the Test Equipment with a short cable (approximately 1m in length).

Procedure:
1. Instruct the Test equipment to transmit a Power via MDI TLV with a PD requested power value different than the previously communicated value.
2. Capture the resulting LLDPDU exchange.
3. Repeat steps 1 and 2 with varying values for PD requested power value.

Observable Results:
The DUT should only change its maximum power draw when it is in sync with the PSE.

Possible Problem: None.