100G Single Lambda PAM4 PMD for 2km SMF

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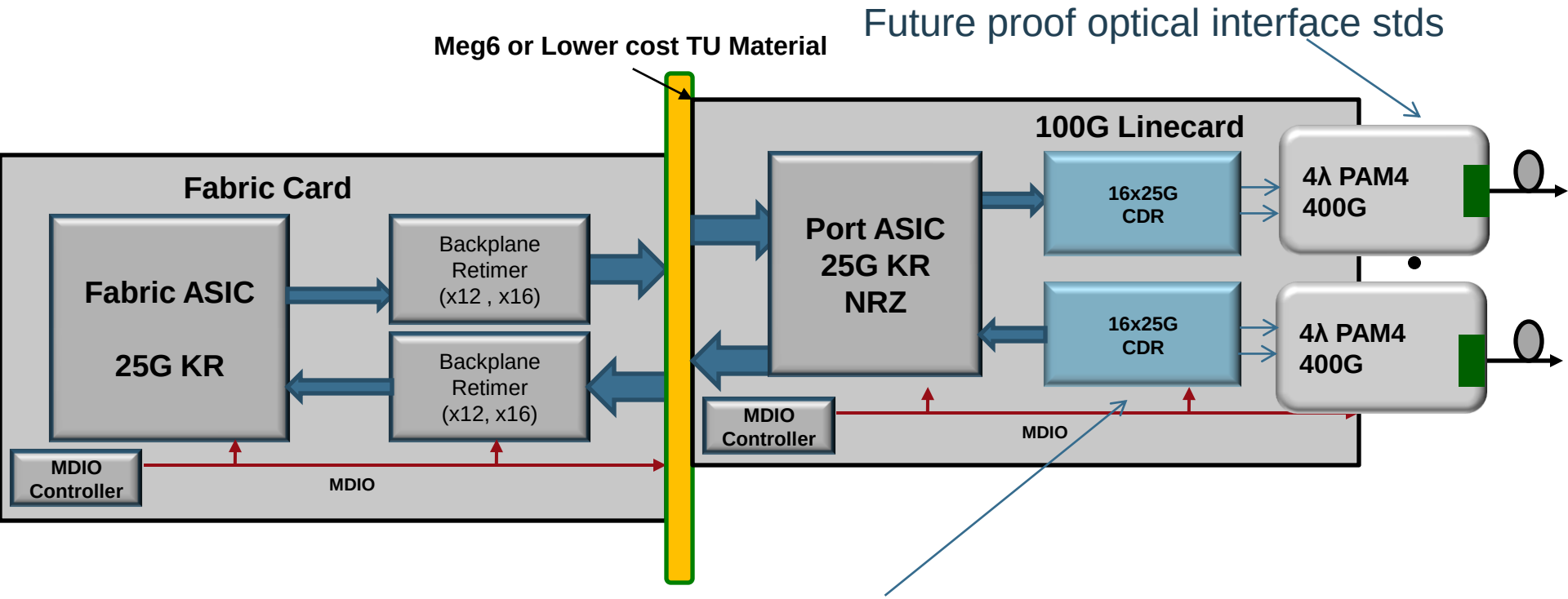
400G using 4λ PAM4

- 400G: Direct Detection 56GBaud PAM4
  - Modulation Speed: 28G → 56GBaud
  - Higher Order Modulation: NRZ → PAM4
  - Single λ Rate: 25G → 100G
  - 4 λ: 100G → 400G

400G System



VSR Electrical Interface : 16x25G NRZ : CDAUI 16

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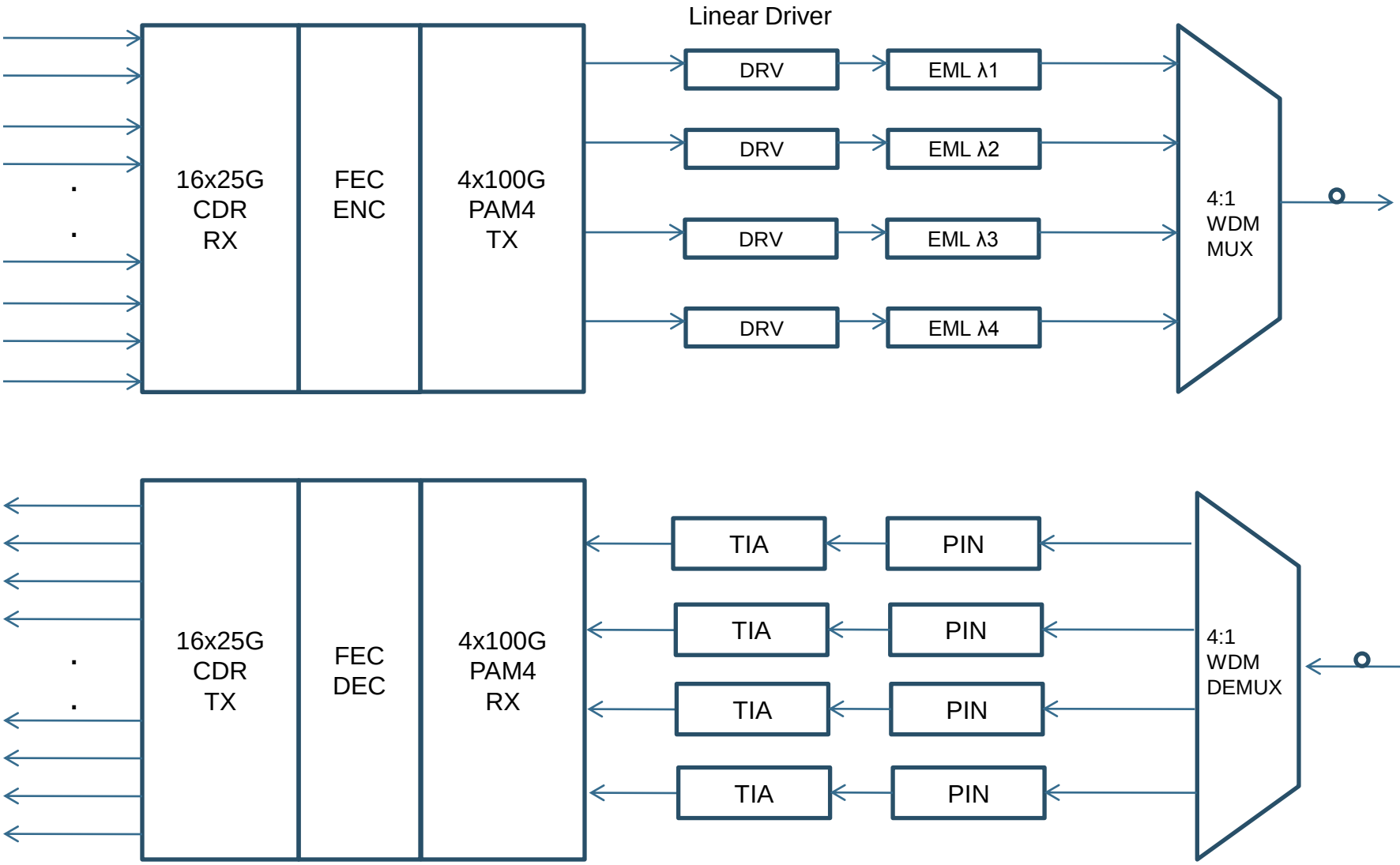
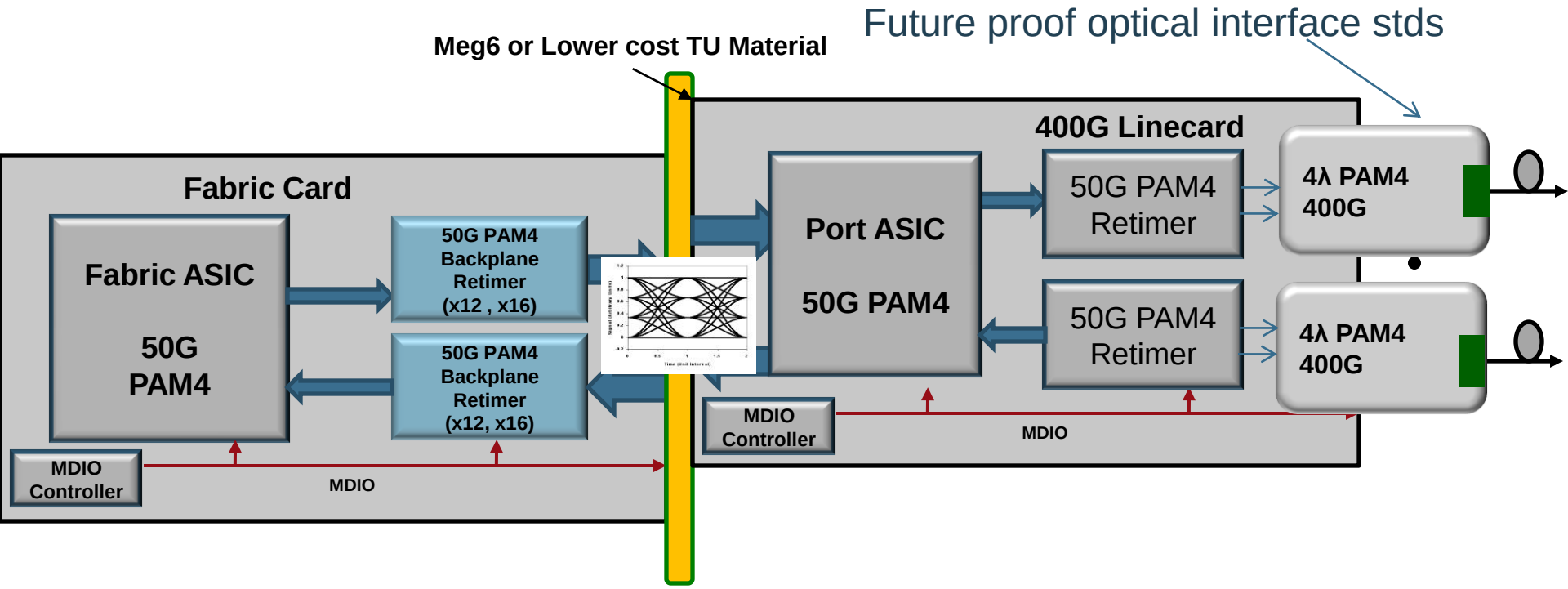
400G Using 4λ PAM4



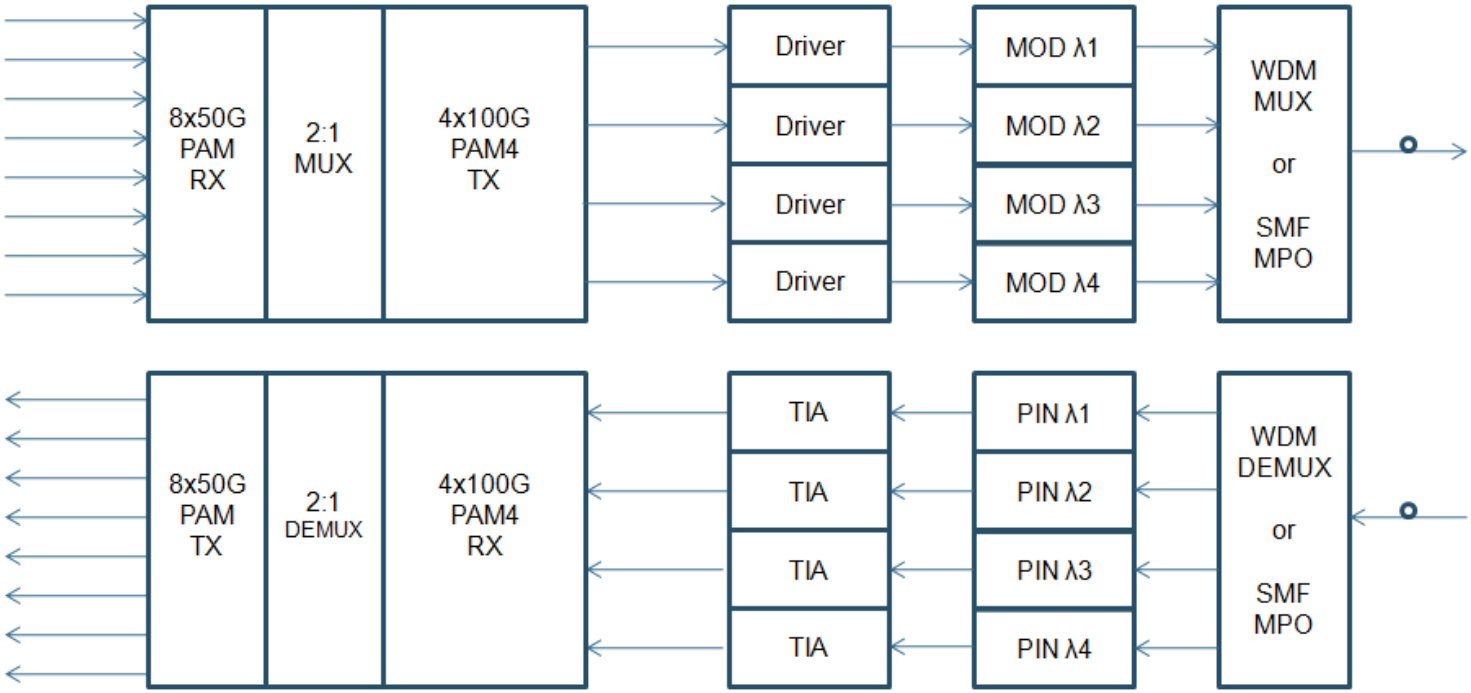
Next Generation Electrical IO



- Backplanes migrate from 25G NRZ to 50G PAM4
  - Reuse PCB, backplanes and connectors

Electrical IO: 16x25G NRZ ⟶ 8x50G PAM4

(100Gx4) 400G 4λ Solution



- 4x100G Optical: 4x (56GBaud PAM4)
- 4x100G Electrical: 8x (28GBaud PAM4)
- Supports 400G uplinks **and** 4x100G leaf and spine breakout

56GBaud PAM4 100Gb/s PAM-4 4λ 400G (4x100G)

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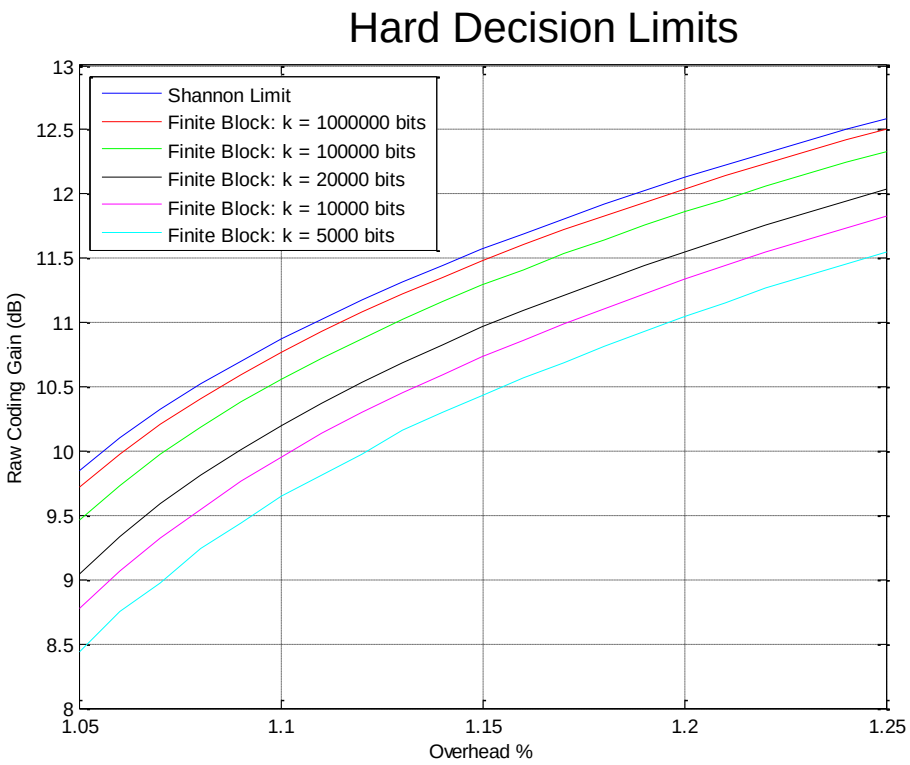
FEC Coding Gain at 1E-15 vs. Overhead



- Hard decision FEC limit is 11dB coding gain for 56GBaud PAM4
  - 12% overhead
  - <100ns latency requirements reduces the coding gain limit to 9dB
- MLC PAM4 codes can provide further coding gain if required

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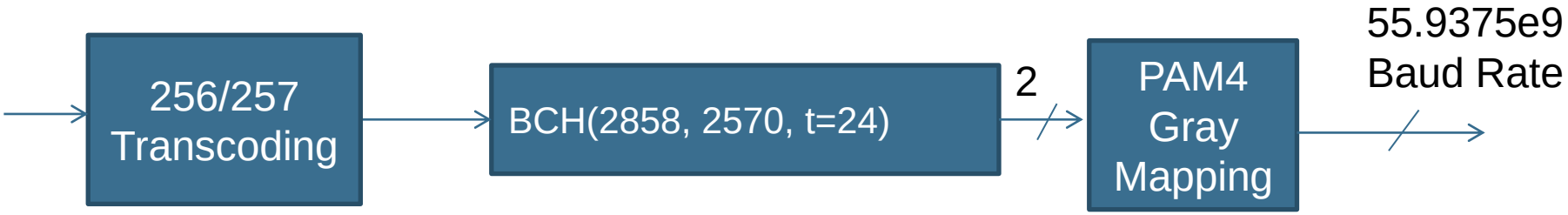
PAM4 FEC proposal with low latency

Choice of FEC code parameters involves a triple tradeoff
– Latency
– Coding gain
– Over clocking (higher Baud rate)

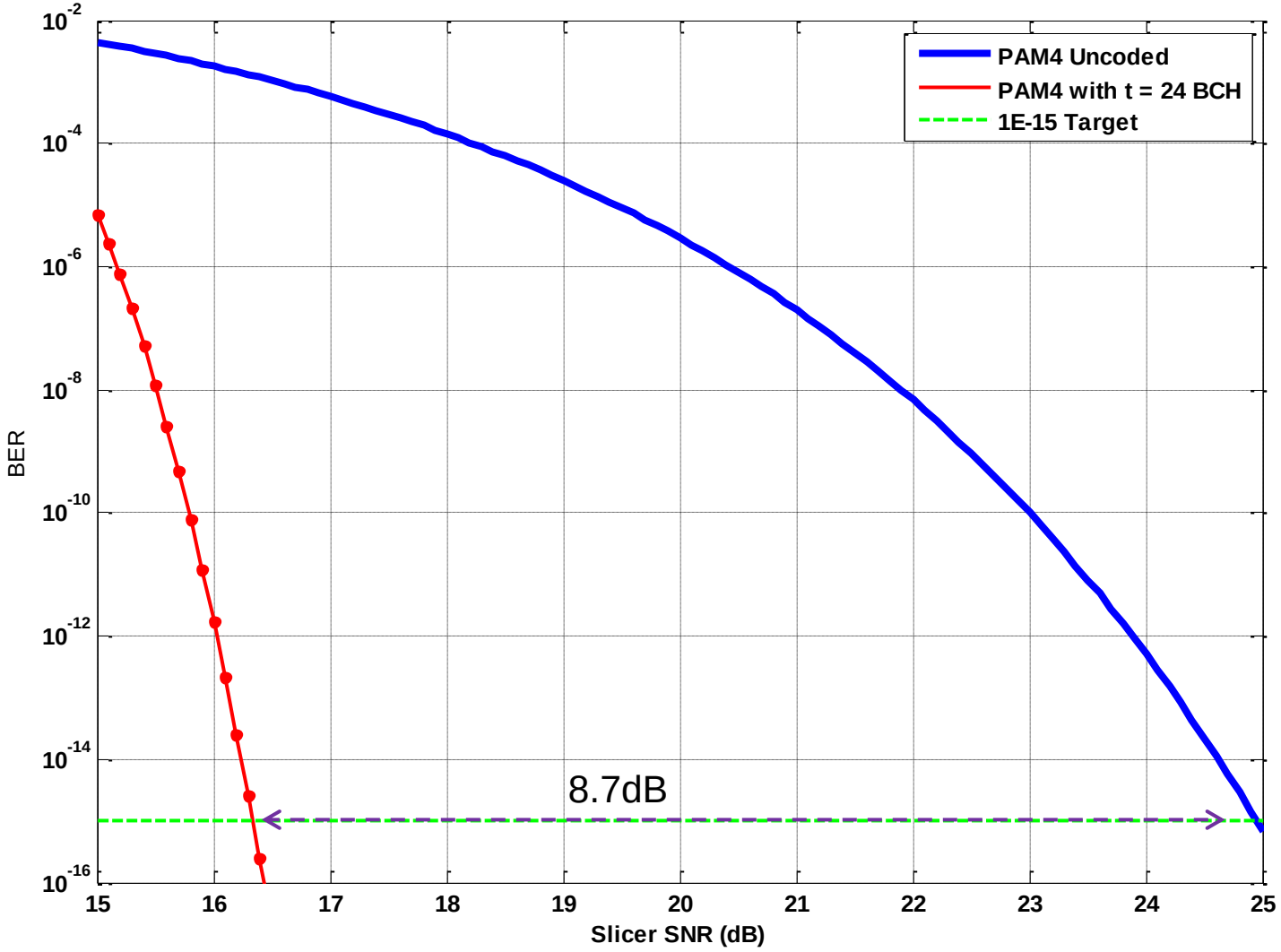


- Gray Mapping, 6 additional parity bits are available.
- Ethernet Rate = 2864 / 2570 * 257/256 * 100 / 2 = 55.9375e9
- Input Error Rate = 1.25E-3, Output Error Rate = 1E-15
- PAM4 SNR = 16.3dB, Coding Gain = 8.7dB

Proposed BCH FEC details

- 100G Intrinsic FEC Block latency is 26ns.
  - 802.3bj KR FEC is 51ns
  - ½ the latency of 802.3bj RS(528,514) KR FEC
- 400G block latency is ~7ns
- Total processing latency is 50ns
  - Processing latency is similar for 100G or 400G.
- Total FEC latency is 75ns, 100ns with error marking
- Rate is 358 x reference clock of 156.25MHz

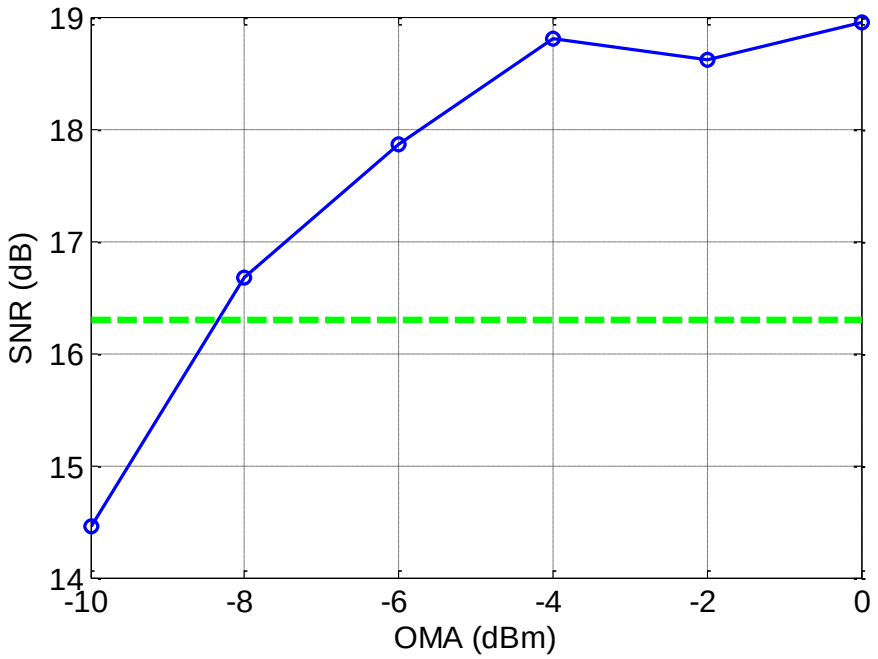
BCH FEC Performance

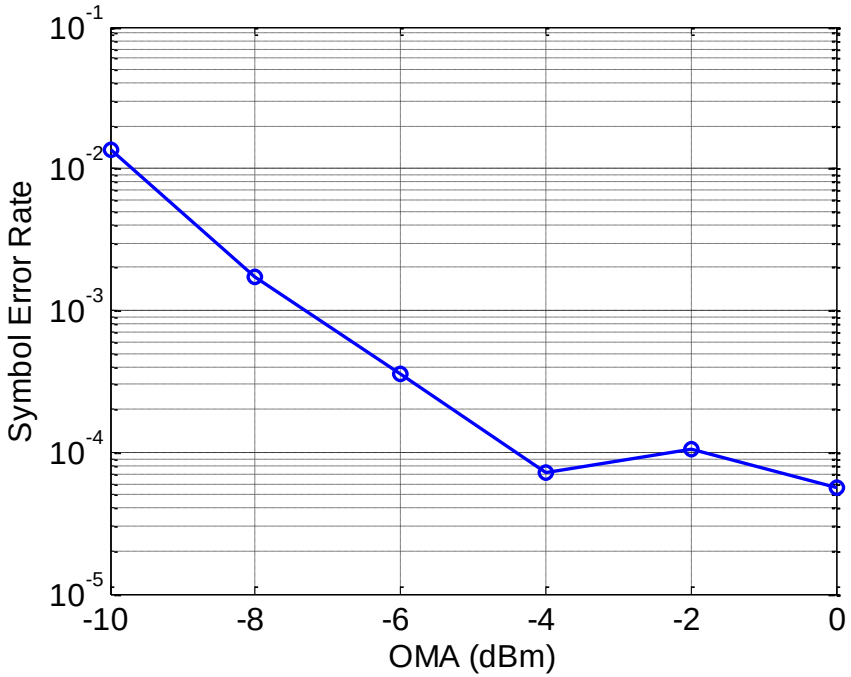


Single Lambda 100G Simulation Parameters

- TIA THD = 3%
- Tx_RJ = 250fs
- Tx_BW = 30GHz
- ER = 6dB
- RIN = -145 dB/Hz
- Resp = 0.9 A/W
- NEP = 20pA/sqrt(Hz)
- TIA_BW = 30GHz
- Rx_RJ = 260fs
- Frequency Offset = 100ppm
- DJ = 2.7ps
- TX Launch OMA = 0dBm
- ADC (1GHz) ENOB = 5.9bits
- ADC (28GHz) ENOB = 4 bits

56GBaud PAM4 Simulation Results





- Sensitivity -8.3dBm for FEC limit
- 1dB loss for 4λ demux
- 4dB link loss budget can be supported

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PAM4 vs. DMT IC Comparison

	PAM4	DMT	Complexity
Equalizer	FFE, DFE	IFFT,FFT	11 taps PAM4, 512 pt FFT/IFFT
Complexity (Multiply-Acc)	x	10x	Dominated by IFFT complex multiplications
DAC resolution	2 bits	8 bits	DMT's QAM64 high ENOB
ADC Power	x	1.5 - 2x	DMT Peak to avg. ratio, QAM64 requires higher ENOB
FEC	x	x	
TIA THD	3%	2%	DMT is more sensitive to non-linearity.
Bandwidth	30G	20G	PAM requires higher BW
Serdes	x	x	
Total IC Power	**Y**	**2.5Y**	

- CMOS Power consumption estimates
  - 1.5W for PAM4, 3.5W for DMT per 100G

Transmitter Characteristics

Parameter		Unit
Electrical Baud Rate (per Lane)	25.78125	
Optical Baud Rate (per Lane)	55.9375	GBd
Modulation	PAM-4	
Wavelengths, nominal	1300	nm
OMA, min	0	dBm
Extinction Ratio, min	6	dB
RIN	-145	dB/Hz
Transmitter reflectance	-35	dB

Transmitter Output Jitter

Parameter	Limit	Test Pattern Condition	Unit
TWDP [1]	TBD	TBD	dBo
Qsq (linear)	32	68.6.7	NA
DCD	0.035	Clock 8 ones/8 zeros	UI
Effective Random Jitter (1 σ) [1, 2]	0.015	PN15 PAM-2	UI
Effective Deterministic Jitter (p-p) [1, 2]	0.15	PN15 PAM-2	UI

1. Waveforms and jitter are captured with reference CDR
2. Effective random jitter and deterministic jitter is the Dual-Dirac fitted parameters with minimum of 64 kbits of samples or equivalent edges

Receiver Characteristics

Parameter		Unit
Rate	55.9375	GBd
Modulation	PAM-4	
Wavelength Range	1300	nm
Rx Avg. Power (max)	2	dBm
Rx Power (min), OMA	-4	dBm
Rx reflectance	-35	dB

Receiver Sensitivity and Jitter Tolerances

Parameter	Limit	Test Pattern Condition	Unit
PAM4 Stressed Receiver sensitivity [1]	-5.5	PN31	dBo
Receiver CDR tracking unstressed	(5, 16)	PN31	(UI, kHz)
Receiver CDR tracking unstressed	(0.5, 160)	PN31	(UI, kHz)

1. Tested with transmitter at the limit of the TWDP with 4 dB of passive loss.

Channel Characteristics

Description	Value	Unit
Operating Distance (max)	2000	m
Channel Insertion Loss (max)	4	dB
Positive Dispersion (max)	1.68	ps/nm
Negative Dispersion (max)	-5.47	ps/nm
Optical Return Loss (min)	28	dB

Summary

- Proposed Optical 56GBaud PAM4
- We have proposed low latency BCH FEC
- BCH BER limit is 1.25E-3 and <100ns low latency
- Simulated 56GBaud PAM4 achieves -8.3dBm
- Proposed specs for 56GBaud PAM4
- Investigated tradeoffs between PAM4 and DMT
- DMT IC power is >2x PAM4 IC power