

Faster – 56Gb/s Standardization Efforts at the OIF

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Agenda

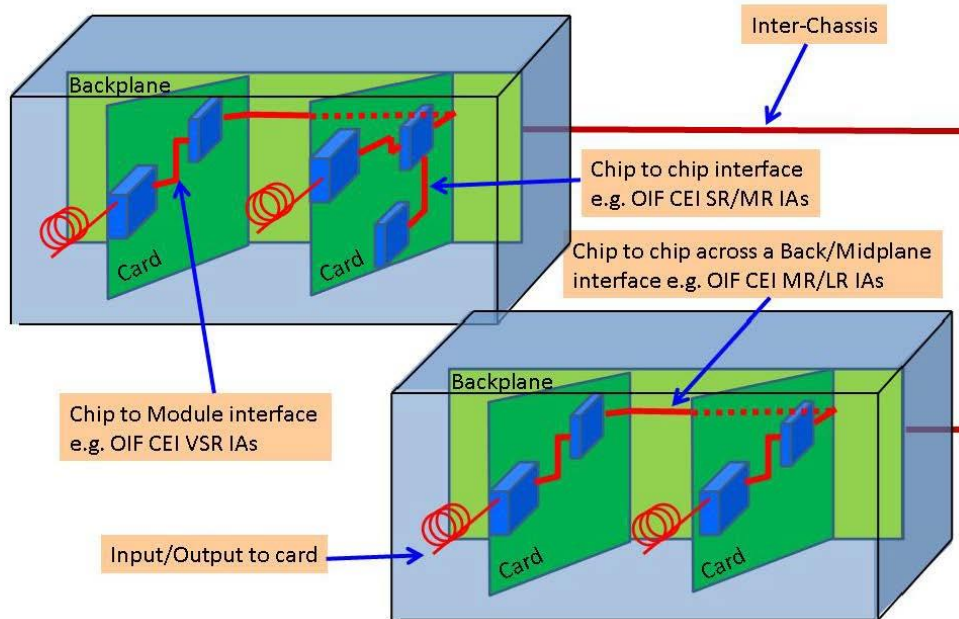
- **OIF efforts on 56Gb/s signaling**
- **Electrical channels being defined**
 - **Physical constraints of reach at higher data rates**
- **Overview of the draft specifications**
 - **Issues being addressed**
 - **Solutions being developed**
- **Summary and Timelines**

OIF Efforts Towards 56Gb/s

- **OIF Physical and Link Layer (PLL) has developed:**
 - **Next Generation Interconnect Framework Document**
 - **Electrical interfaces for client side**
 - **Links from 10mm up to 2km**
 - **Electrical & Optical**
- **OIF PLL is currently working on:**
 - **Specific projects for next generation interoperable electrical interfaces**

CEI Application Space is Evolving

- ◆ The “OIF Next Generation Interconnect Framework” white paper lays out a roadmap for CEI-56G serial links
- ◆ 2.5D and 3D applications are becoming increasingly relevant
 - ◆ High function ASICs (such as switch chips) are driving requirements for higher I/O density and lower interface power
 - ◆ Chip-to-chip and mid-plane interfaces are becoming more relevant than high loss backplanes (at least in the near-term)



- ◆ Overall themes emerging:
 - ◆ Pin density is not increasing fast enough for high density ASICs
 - ◆ Power reduction of 30% from one generation to next is not good enough

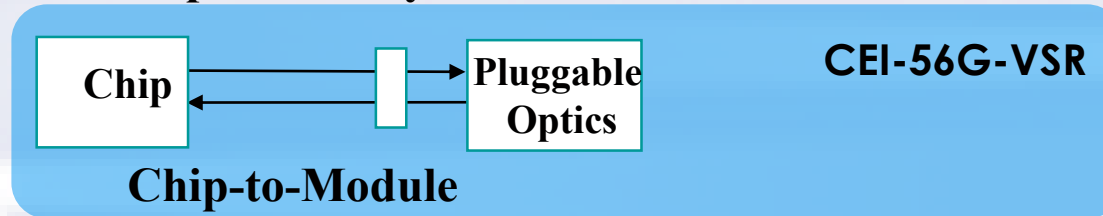
CEI-56G Application Space



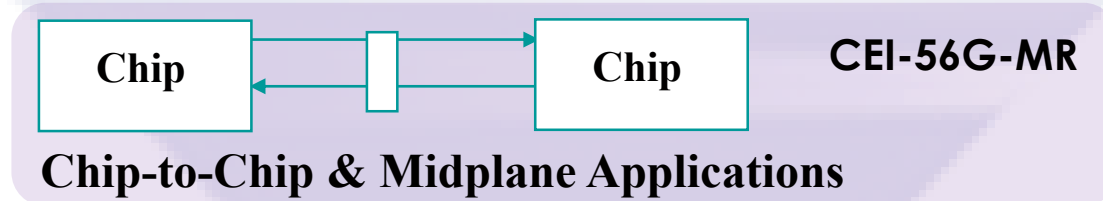
- ❖ **USR: 2.5D/3D applications**
 - ❖ 1 cm, no connectors, no packages



- ❖ **XSR: Chip to nearby optics engine**
 - ❖ 5 cm, no connectors
 - ❖ 5-10 dB loss @28 GHz



- ❖ **VSR: Chip-to-module**
 - ❖ 10 cm, 1 connector
 - ❖ 10-20 dB loss @28 GHz



- ❖ **MR: Interfaces for chip to chip and midrange backplane**
 - ❖ 50 cm, 1 connector
 - ❖ 15-25 dB loss @14 GHz
 - ❖ 20-50 dB loss @28 GHz



- ❖ **LR: Interface for chip to chip over a backplane**
 - ❖ 100cm, 2 connectors
 - ❖ 35dB at 14Ghz

56Gb/s Themes Emerging

□ Limitations

- PCB loss characteristics at higher data rates
- Power consumption limits at the chip and line card levels

□ Methods other than NRZ signaling

- PAMx, Chord Signaling, DMT, etc
- Higher Order Modulation can gain more bits per clock cycle, allowing lower baud rates

□ Alternative architectures

- Orthogonal structures
- Lower loss materials such as “cable”
- Mid board optics

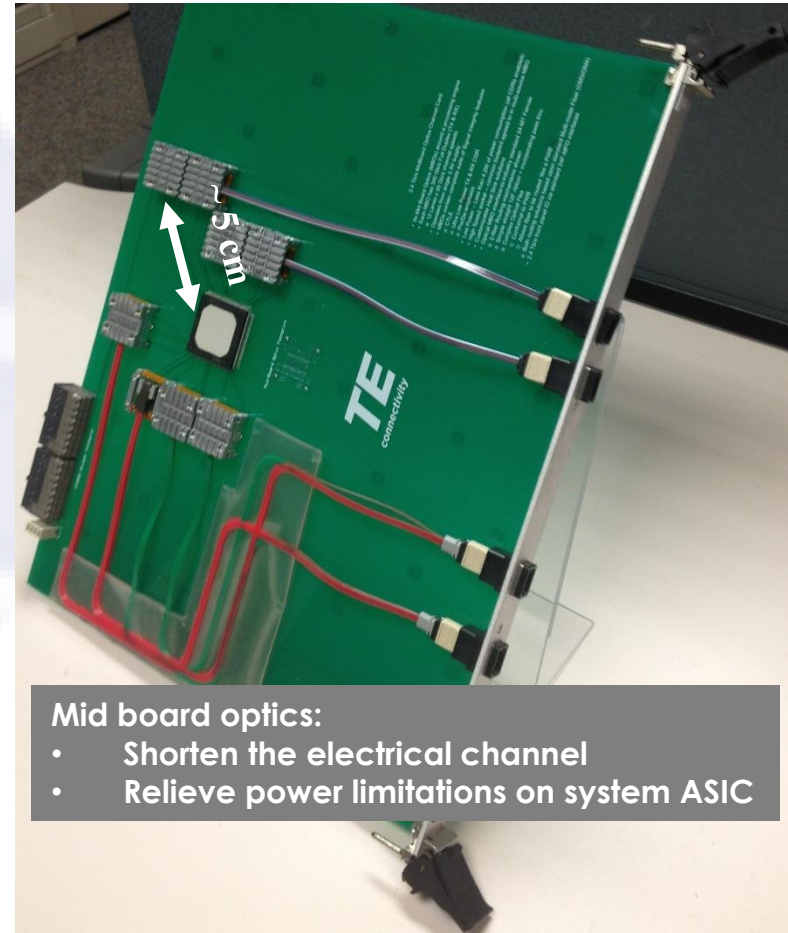
Industry needs to agree on path forward to maximize interoperability



OIF OPTICAL
INTERNETWORKING
FORUM

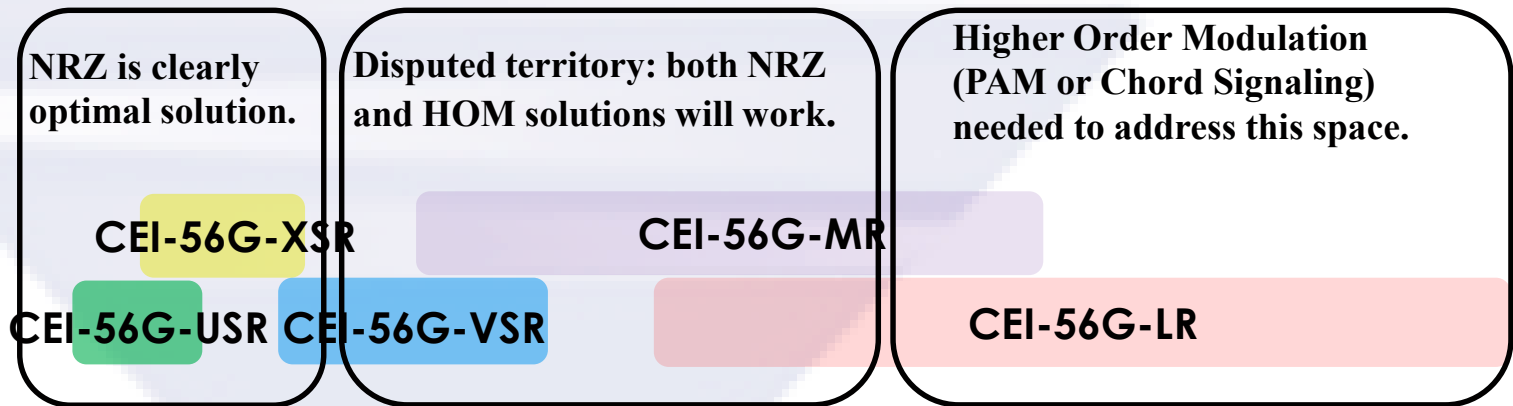
Market Bifurcation

- Application space for prior generations consisted of SR, VSR, MR, LR applications.
 - Similar signaling solution was used for the entire range of applications
 - Common SerDes design was often used, especially on early products
- Chip power limitations for large ASICs is forcing LR/MR SerDes function off chip.
 - Signaling for MR/LR may be different from lower loss applications
 - Substantially different SerDes designs with substantial power reduction are required for USR/XSR applications as compared to MR/LR applications
- Advanced signaling will likely be required for MR/LR applications at 56 Gb/s.
 - NRZ not viable at losses above 36 dB
 - Most easily achievable channel design improvements were already deployed to support 25 Gb/s
 - Higher order modulation (PAMx, Chord Signaling, etc.) will be needed to support high loss applications at 56 Gb/s and up



CEI-56G Solution Options

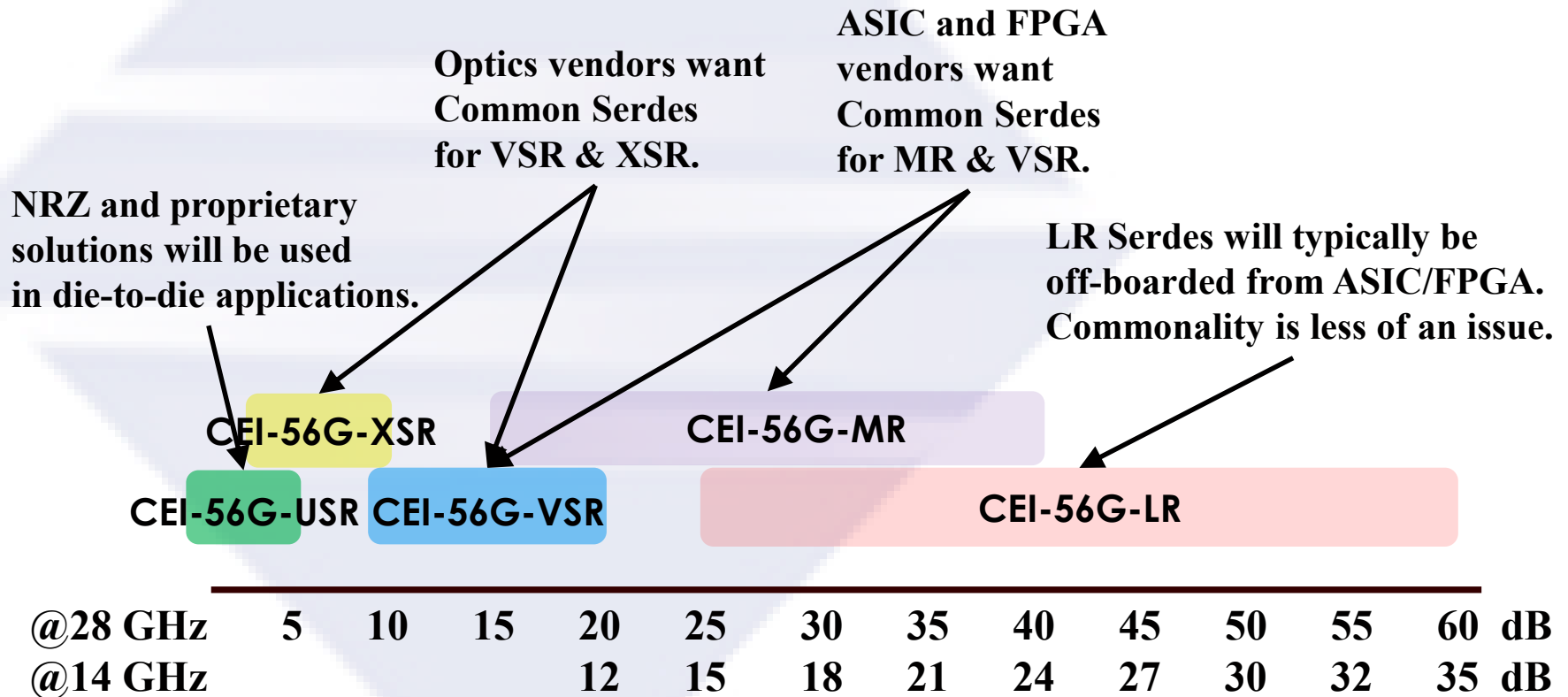
- ◆ OIF contributions have considered various signaling solutions for these application spaces:
 - ◆ NRZ – optimal power and complexity solution for lower loss applications but not feasible at higher loss ranges.
 - ◆ PAM4 – reduces Nyquist frequency, supporting higher loss ranges.
 - ◆ Chord Signaling – Also reduces Nyquist frequency, supporting higher loss ranges.



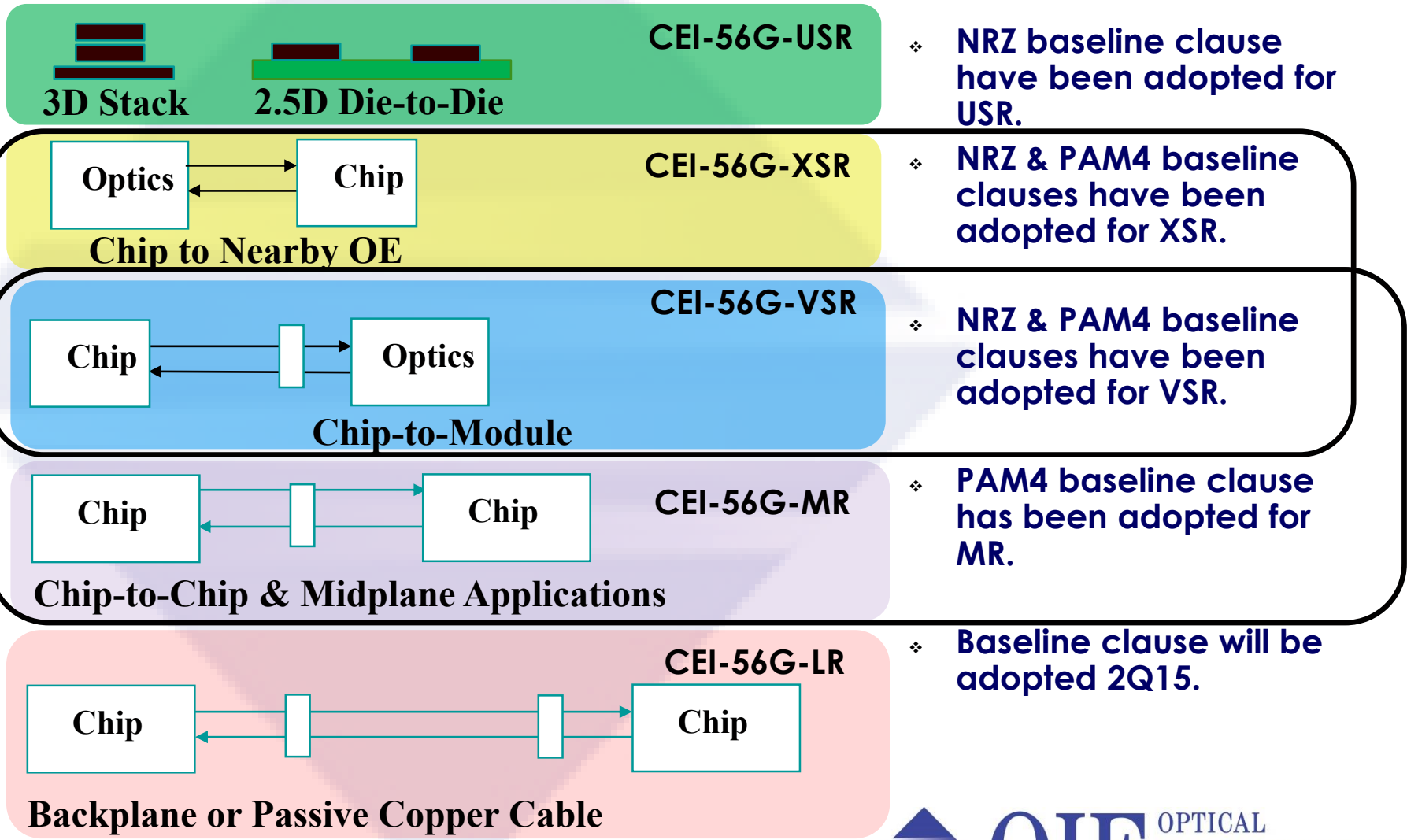
@28 GHz	5	10	15	20	25	30	35	40	45	50	55	60 dB
@14 GHz				12	15	18	21	24	27	30	32	35 dB

CEI-56G Serdes Commonality

- ◆ **Push for Serdes commonality between application spaces has been driving factor for baseline text adoption.**



CEI-56G Baseline Clauses



Summary

- **Six draft implementation agreements are in process**
 - **NRZ: USR, XSR, VSR**
 - **PAM4: XSR, VSR, MR**
 - **LR does not yet have a draft started yet**
- **Projected timelines:**
 - **Quarterly liaisons planned to IEEE 802.3bs project**
 - **Technically stable documents (no TBDs) in early 2015**

Thank You

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