50Gb/s Per Lane: The Next Technology Rate

The Rate Debate

Technology Exploration Forum

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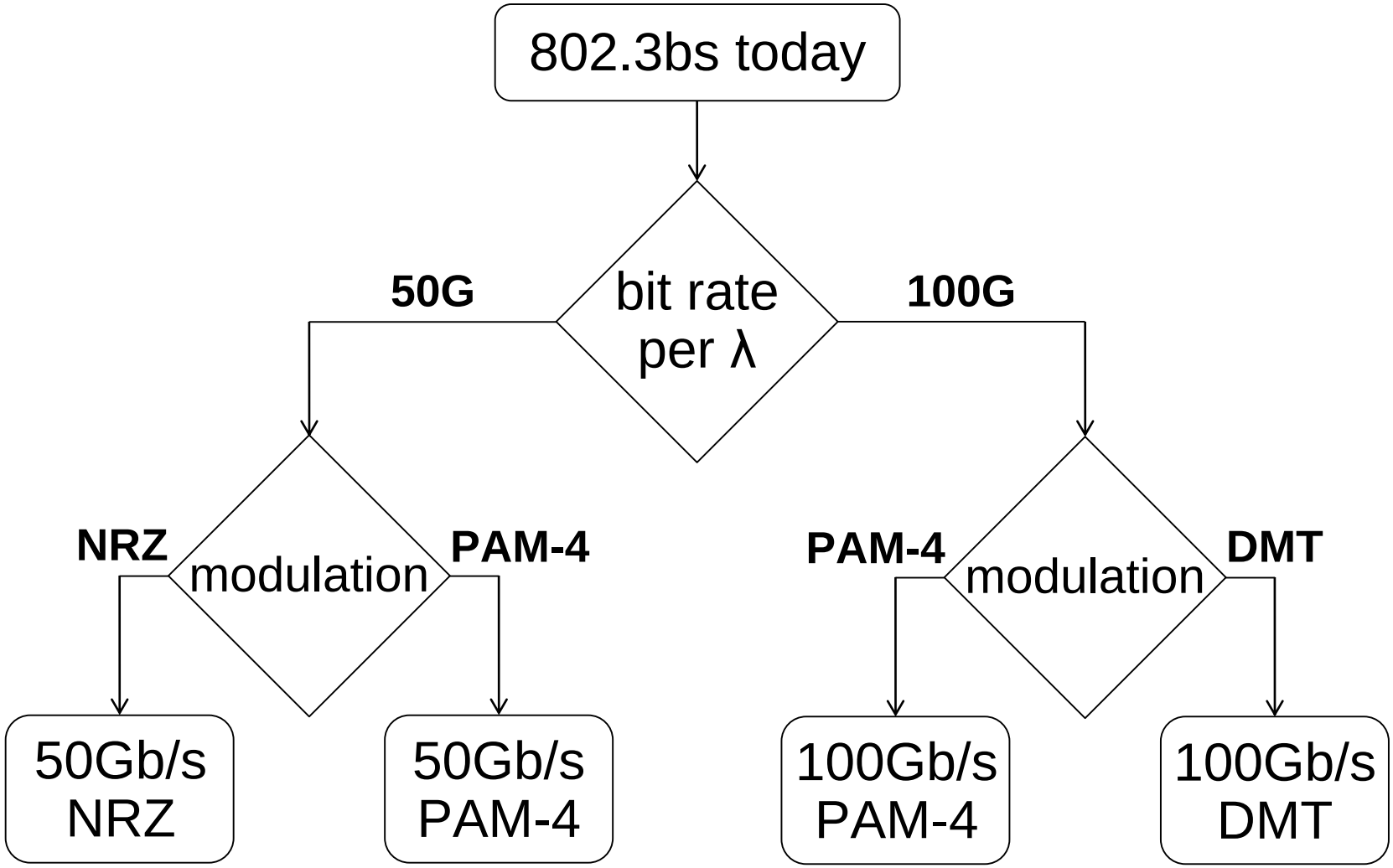
Technology Exploration Forum

Finisar®

IEEE 400G Ethernet Rate/Modulation Debate



Historical Rate Progressions

Data Rates Gb/s:

- Telecom:

  0.16 → 0.62 → 2.5 → 10 → 40 → ~~160~~ → 100 → 400/Flex

- Ethernet

  1 → 10 → 100 → 40 → 400 → 25 → 2.5/5.0 → 50

- Storage (Fibre Channel)

  1 → 2 → 4 → 8 → 16 → 32 → 128 (4x) → 64

- InfiniBand (4x)

  32 → 56 → 100 → 200

Mainstream Technology Lane Rates Gb/s:

- 1 → 2.5 → 5 → 10 → 25 → 50

Historical IEEE Ethernet SMF λ Rate Debates

Ethernet Rate	10G	40G	100G	400G
Task Force	802.3ae	802.3ba	802.3ba	802.3bs
Project years	1999-2002	2006-2010	2006-2010	2013-
Existing optics	OC192	OC768	OC768	LR4
Existing λ rate	10G/λ	40G/λ	40G/λ	25G/λ
Existing I/O rate	2.5G (3G)	10G	10G	25G
Predicted next I/O (SerDes) rate	10G	25G	25G	50G
λ rate debate	**4x3G/λ v. 1x10G/λ**	**4x10G/λ v. 1x40G/λ**	**10x10G/λ v. 4x25G/λ**	**8x50G/λ v. 4x100G/λ**
Market Winner	10G/λ	10G/λ	25G/λ	50G/λ

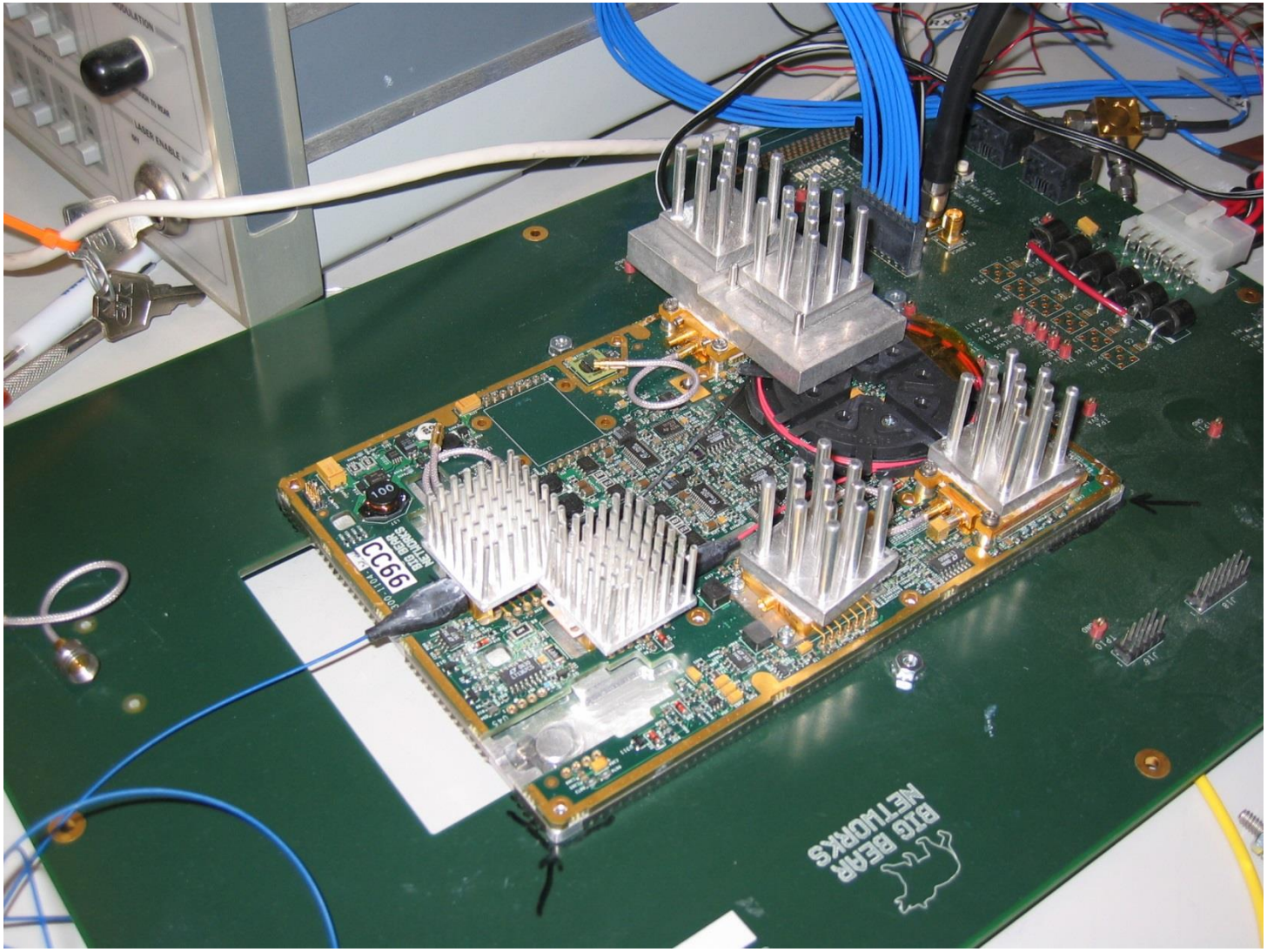
802.3 SMF PMD λ Rate Debates Observations

- 802.3 λ rate debates were always between rates in existing client optics
- 802.3bs SMF PMD λ rate debate breaks this precedent by considering rate (100G/λ) not in existing client optics
- 802.3ae 10G SMF PMD λ rate debates:
  - adopt existing vs. next I/O (SerDes) rate for optics
- 802.3ba 100G SMF PMD λ rate debates:
  - adopt existing vs. next I/O (SerDes) rate for optics
- 802.3ba 40G SMF PMD λ rate debate:
  - adopt existing vs. many years out I/O (SerDes) rate
  - 40G/λ argument: 1 laser is low cost & CMOS is free
- 802.3bs 400G SMF PMD λ rate debate
  - adopt next vs. many years out I/O (SerDes) rate
  - 100G/λ argument: 4 lasers are low cost & CMOS is free

40G Serial Example of Premature Standard

- 40G Serial Client OC768 and G.693 spec. in late 90s
- Based on assumption that client interfaces should be serial
  156M → 622M → 2.5G → 10G → 40G
- Bleeding edge component limitations drove specifications
  Ex. -5dBm RX sensitivity limit resulted in bad specs.
  - 1550nm λ
  - 1dB CD Penalty
  - Required changing CD penalty after many years of futile attempts to make production parts
- Nightmare to design and manufacture modules
  - Transistor fT = 110GHz
  - Interconnect technology: GPPO
  - Packaging technology: gold boxes for optics and ICs
- Today's 100G/λ technology is similarly bleeding edge

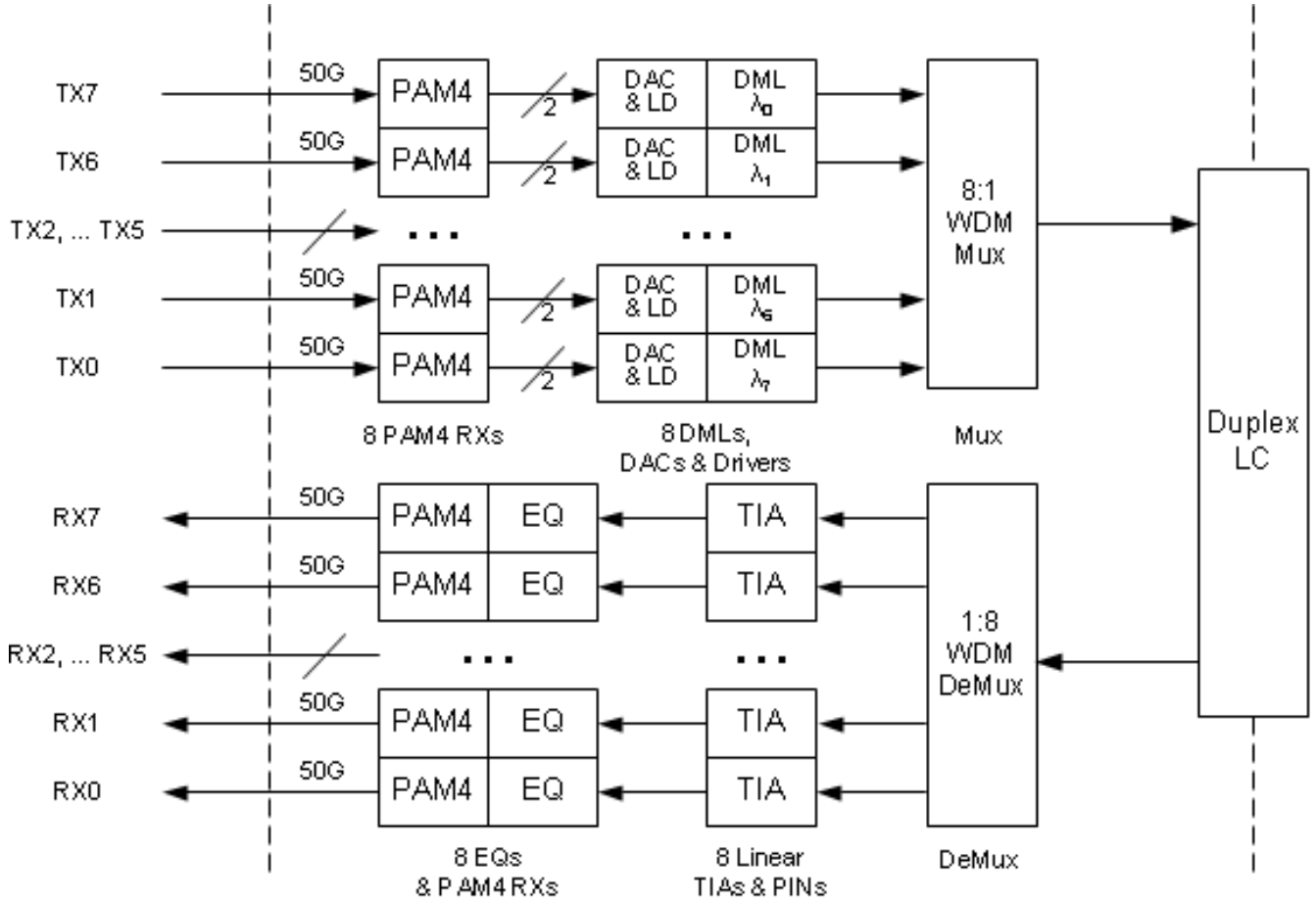
1st 40G Serial Module on Eval Card c. 2003



Next Technology Rate Application Feasibility

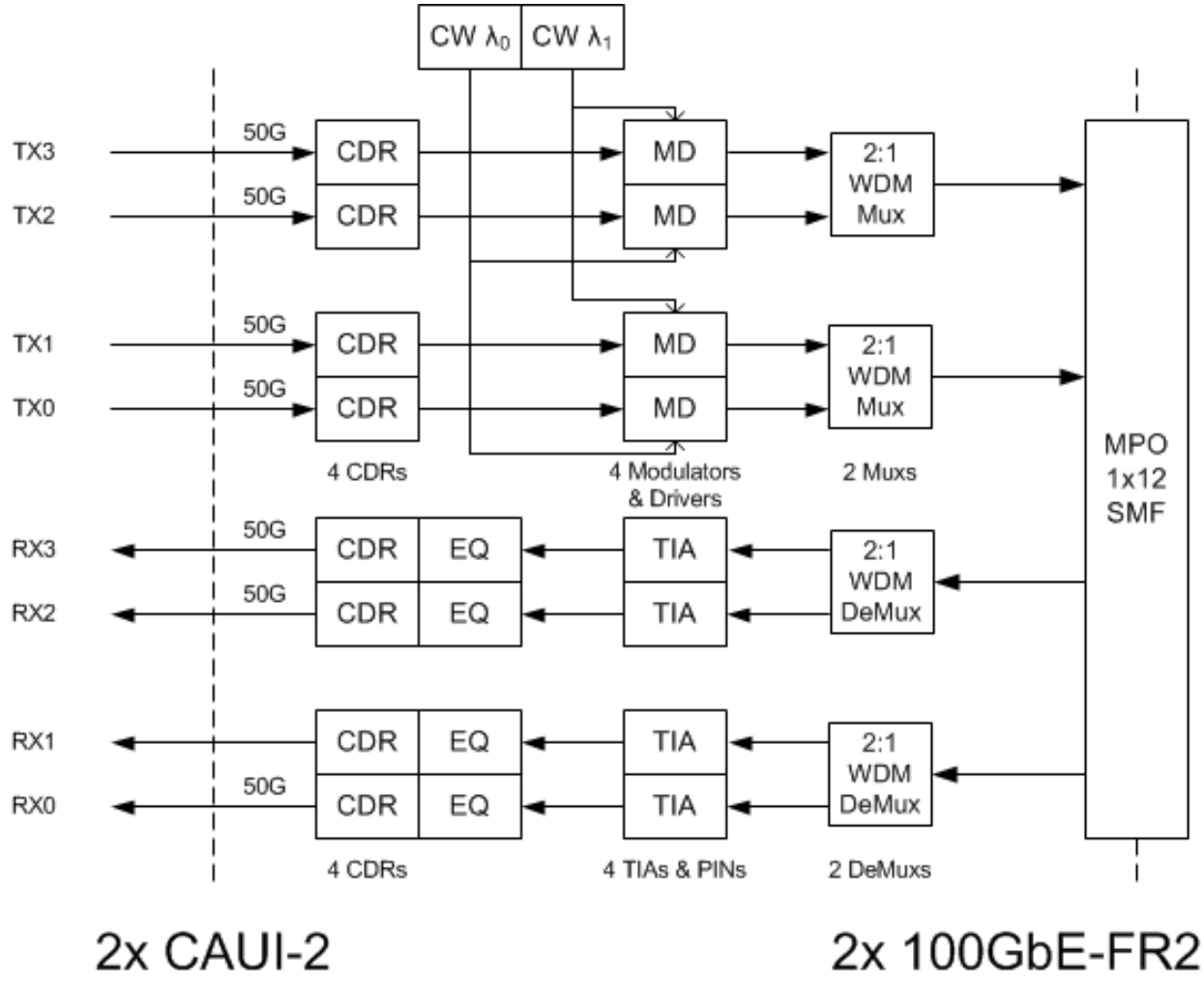
Application Support Feasibility	50G NRZ or PAM-4	100G PAM-4 or DMT
400G 10km & High-Loss duplex SMF	Yes	No
400G 2km duplex SMF	Yes	No
400G 500m PSM4	Yes	Yes
400G Next Gen MMF	Yes	No
100G Next Gen SMF	Yes	Yes
100G Next Gen MMF	Yes	No
50G Serial SMF & MMF	Yes	No
40G Serial SMF & MMF	Yes	No
64x Fibre Channel	Yes	No
50G per lane Electrical I/O	Yes	No
50G per lane Backplane & Cu Cable	Yes	No

400G (8x50G λ) SMF PMD Example



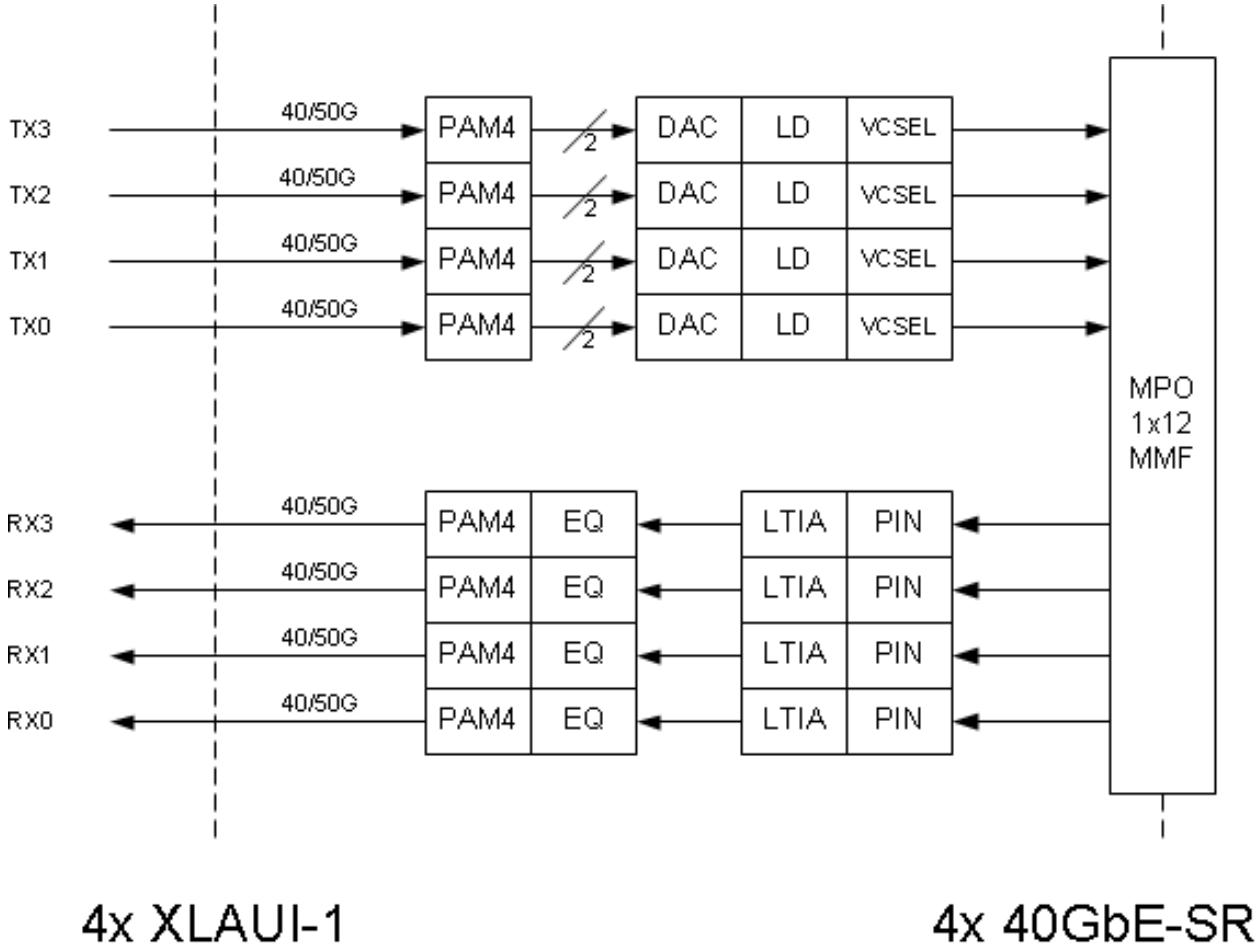
- CFP2 400G module

200G (2x 2x50G λ) SMF PMD Example



- QSFP & CFP4 dual 100G module

40/50G (Serial λ) MMF PMD Example

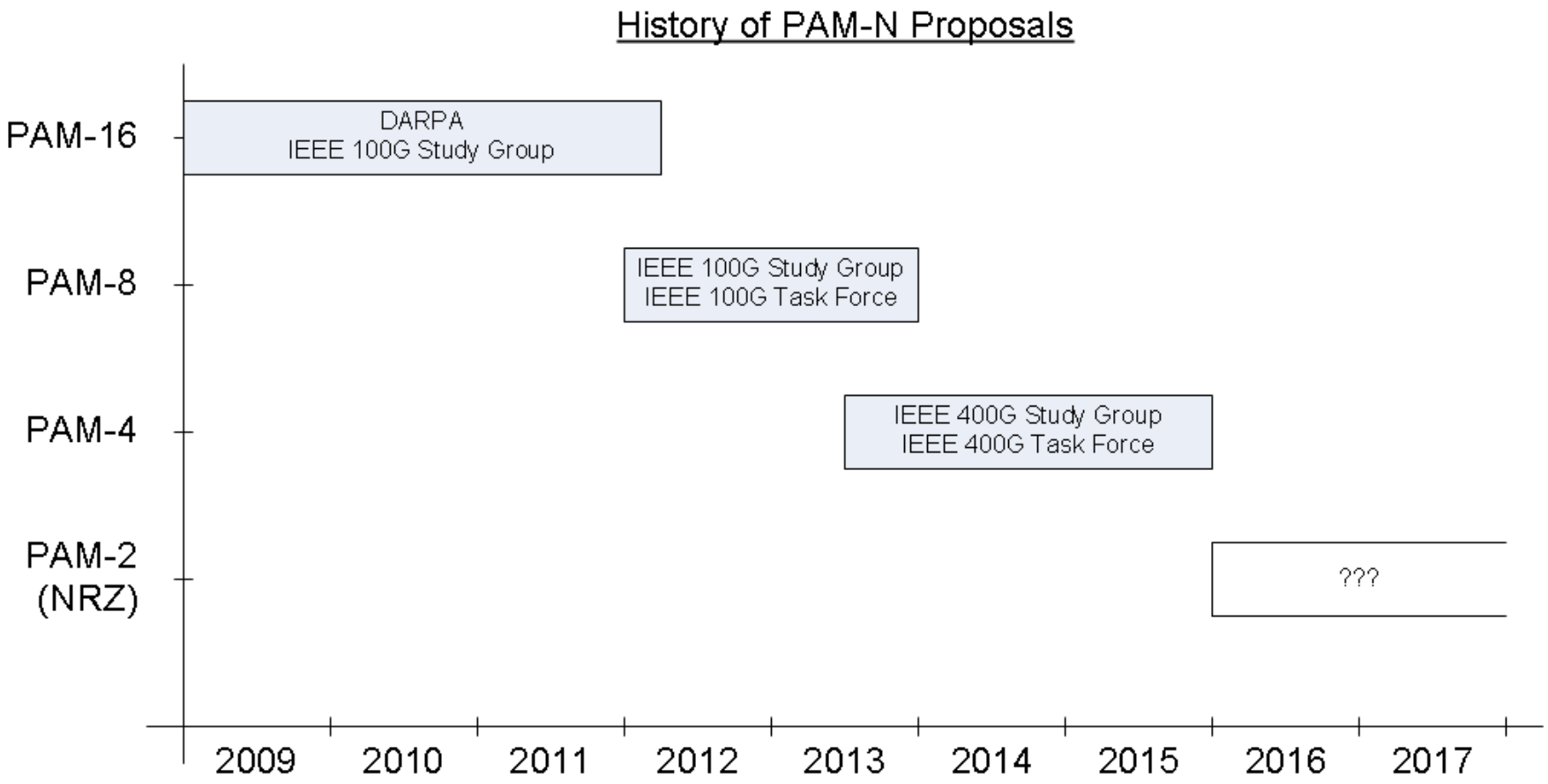


- QSFP quad 40/50G (160/200G) module
- SFP 40/50G single lane module

100G SMF PMD Power

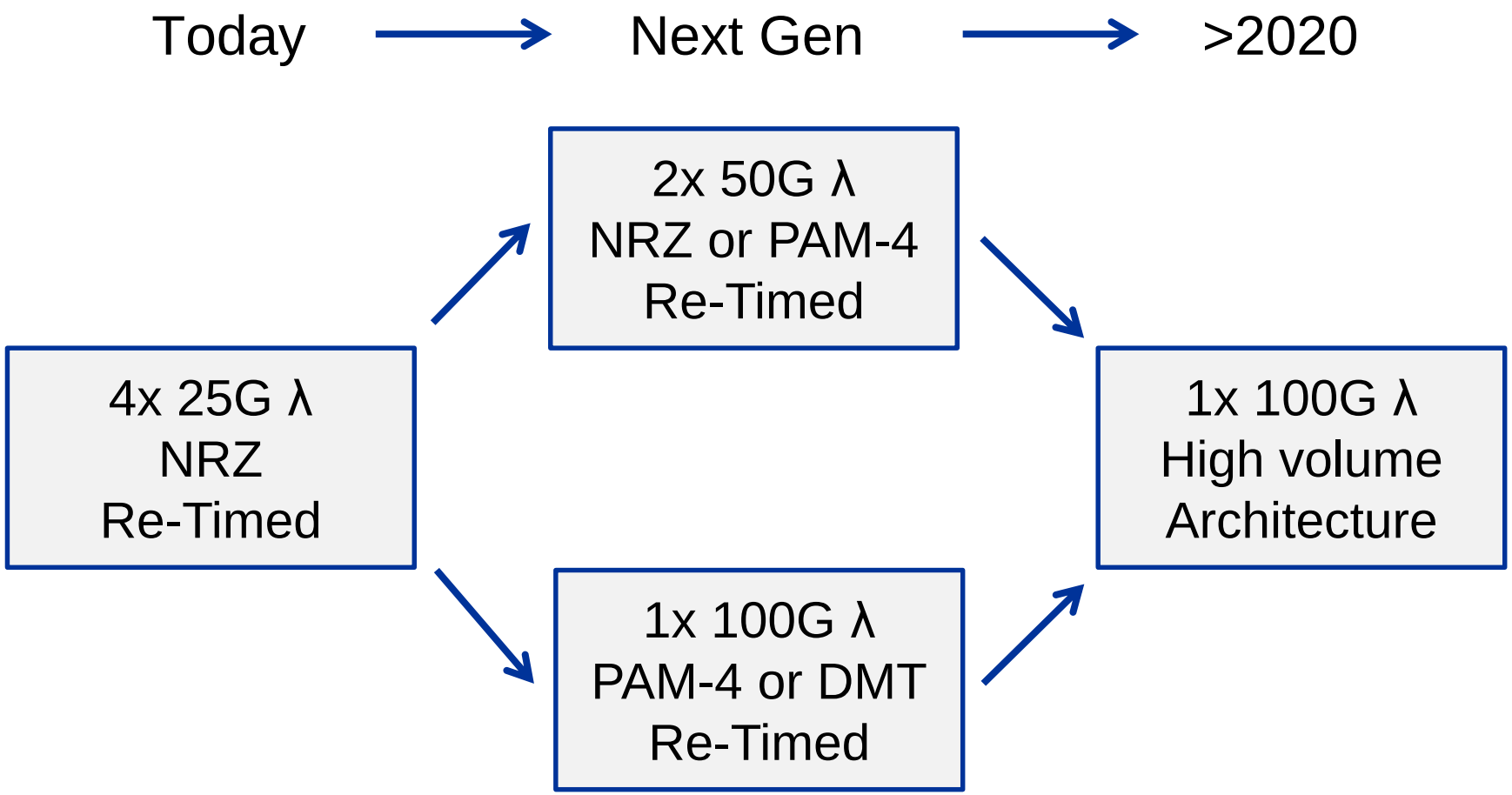
- Gen 1 LR4 CFP discrete EML: 20W
- Gen 2 LR4 CFP2 DML or MZ: 6W
- Gen 3 LR4 CFP4 DML: 4W
- Gen 4 LR4 QSFP28 DML: 3.5W
- Gen 4 CWDM4 QSFP28 DML: 3W
- Next Gen CWDM2 (2x50G/λ) MZ or DML Target: 2W
  - Enables dual 100G (200G) QSFP and CFP4
- Current 100G/λ proposals, even w/ advanced CMOS, at best match power of current LR4 or CWDM4 QSFP28
  - Not compelling
- 100G/λ Compelling Target: 1W
  - Enables 100G SFP and quad 100G CFP4 and QSFP

Example of Fast Changing Technology



Cautionary note: adopting PAM-8 Baseline Proposal in 802.3bm would have been premature

100G/400G Standards Today are for >2020



Track record of predicting technology many years our is poor

50G/λ is the Right Next Step

- Same reason that crooks rob banks:
  - It's where the money is
  - Equivalently it's where the volume is
- Manageable optics technology risk
- Leverages next high-volume mainstream technology rate
- Optimally connects to 50G I/O
- Multiple applications that drive shared volume
  - 400G SMF & MMF
  - 2x density increase duplex SMF and MMF 100G
  - 4x density increase duplex SMF and MMF 40/50G
  - 64xFC
- Technology is sufficiently understood to standardize

100G/λ is >2020 Solution

- Standardization today is premature
  - Bleeding-edge optics negate architecture advantage
  - No power advantage over today's approach (4x25G/λ)
  - Skips next high-volume mainstream I/O rate (50G)
  - Niche application and rate for many years (>2020)
- Standardization will be done in the future when there is:
  - Optics experience
  - Mature components
  - Compelling power (ex. 1W/100G)
  - 100G electrical I/O architecture and volume visibility
  - Multiple application volume to drive down cost
- Best way to derail promising advanced technology is to lock down today's incomplete understanding in a standard

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Thank you