Gen 2 PoE Certification Program Test Plan
Version 1.4

Ethernet Alliance

November 17, 2020

Notice

THIS POE TEST PLAN IS PROVIDED "AS IS" WITH NO WARRANTIES WHATSOEVER, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, FITNESS FOR ANY PARTICULAR PURPOSE, OR ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, POE TEST PLAN, OR SAMPLE.

The Ethernet Alliance and its members disclaim all liability, including liability for infringement of any proprietary rights, relating to use of information in this PoE Test Plan. Use and implementation of this PoE Test Plan may be subject to patent rights of third parties, including both persons who have contributed to the PoE Test Plan and persons who have not contributed to it, and both members and non-members of the Ethernet Alliance. THE ETHERNET ALLIANCE MAKES NO REPRESENTATIONS OR WARRANTIES AS TO THE EXISTENCE OR ABSENCE OF SUCH RIGHTS AND SHALL HAVE NO RESPONSIBILITY, OBLIGATION, OR LIABILITY TO ANY PERSON, IN ANY MANNER OR CIRCUMSTANCE, UNDER ANY LEGAL THEORY WHATSOEVER, FOR FAILURE TO RECOGNIZE, DISCLOSE, OR IDENTIFY ANY PATENT RIGHTS OR ANY OWNERS OR CLAIMANTS THEREOF; FOR ANY INCOMPLETE OR INACCURATE IDENTIFICATION OR DISCLOSURE OF SUCH RIGHTS, OWNERS, OR CLAIMANTS; OR FOR YOUR OR ANY PERSON'S RELIANCE ON OR USE OR IMPLEMENTATION OF THE POE TEST PLAN OR INCORPORATION THEREOF IN TEST TOOLS OR TEST EQUIPMENT, PROTOCOLS, SOFTWARE, OR TESTING PROCEDURES OR OTHER PRODUCTS.

This PoE Test Plan may also incorporate by reference other specifications published by third parties. Any licensee of this PoE Test Plan is solely responsible for acquiring any licenses from such third parties that are necessary to access, use, and/or implement such third parties' PoE Test Plans.

History of changes

This document is Version 1.4, dated November 17, 2020.

Changes to improved and updated versions of this document are recorded here in the Tables below. These changes are the result of accepted comments filed against the testplan. The "ID" column in the change Tables is an identifier for the comment that caused a particular change. The description of the change is meant to be informative rather than exhaustive, carefully check the precise differences made by comparing to the previous version of the test plan.

Version 1.0

This is the initial release of the Test Plan.

Version 1.1

The following changes were made compared to the previous release of the testplan.

ID	Section	Page	Description of change
2	9.70.1	141	Test re-written and parameters changed for clarity and repeatability.
3	9.70.2	142	Test re-written and parameters changed for clarity and repeatability.
4	12.2	295	Modified test to allow it to be run independently of 12.1 by making the test model send an first frame with initialized power values.
5	9.11	65	Better handling of the case where negative detection currents are measured during a test.
6	9.64	130	Fixed the pin numbering in Figure 9.
7	9.64	130	Added a high pass filter to the measurement circuit in Figure 9 to make the test insensitive to PD load changes.
8	11.64	271	Fixed the pin numbering in Figure 10.
9	11.64	271	Added a high pass filter to the measurement circuit in Figure 10 to make the test insensitive to PD load changes.
10	9.24a	80	Added a test for a new Autoclass requirement in IEEE P802.3cv.

Version 1.2

The following changes were made compared to the previous release of the testplan.

ID	Section	Page	Description of change
9	11.64	271	Comment #9 against version 1.0 was not implemented correctly. The measurement circuit in Figure 10 was modified to include a highpass filter and the measurement below 500 Hz was removed.

Version 1.3

The following changes were made compared to the previous release of the testplan.

ID	Section	Page	Description of change
11	9.24	80	Clarify reference to IEEE 802.3cv maintenance
12	11.51	245	Include a second inrush test procedure and changed pass requirements to require passing one of the two test procedures
13	11.61	263	Modified current limit test procedure to improve testability
14	11.62	267	Modified current limit test procedure to improve testability
15	11.63	270	Modified test procedure to mark the test "No test required" and remove procedure from test plan

Version 1.4

The following changes were made compared to the previous release of the testplan.

ID	Section	Page	Description of change
16	3	295	Modified PD DLLC test procedures to add a 5 minute delay after an Ethernet link is established

Contents

1 Overview of the program

The EA PoE Certification Program is an Ethernet Alliance Defined Program to provide branding for IEEE 802.3 PoE Products. This branding includes both a visible logo for use on products and a listing on an EA Certified Products website with all relevant product information.

This program is designed to differentiate products that comply to IEEE 802.3 Power over Ethernet from other products that market themselves as Power over Ethernet.

The program is designed to be open, lightweight, and as simple as possible administratively. It supports both first- and third-party testing. Certification covers complete systems, including evaluation systems. It will not certify individual components. Logos are based on single port per product testing but does not preclude testing on all ports.

The Ethernet Alliance will institute both brand protection and conflict resolution processes for disputes relating to the logo program.

2 Device information provided

In order to perform the correct test procedure the following information is provided with each device that is being tested.

2.1 Required information for PSE tests

Type of the PSE, which can be Type 3 or Type 4.

Highest Class the PSE is able to support, this can be any of 1 through 8.

4-pair capability indicates the PSE is capable of providing power over 4-pairs. A PSE capable of 4-pair operation is referred to as a “4-pair PSE”, a PSE that can only operate over 2 pairs is referred to as “2-pair PSE”.

PSE evaluation system indicates that the PSE is an evaluation system.

DLL capability indicates that the PSE supports the Power via MDI TLV and Data Link Layer classification.

The PSE’s Logo Class is determined to be the highest Class the PSE is able to support.

2.2 Required information for PD tests

Type of the PD, which can be Type 3 or Type 4.

Signature configuration which can be single-signature or dual-signature.

Requested Class of the PD, which can be any of Class 1 through Class 8 for single-signature PDs, and any of Class 1 through Class 5 for each Mode of the dual-signature PD. For a dual-signature, the requested Class for both Mode A and Mode B must be provided.

Link speeds that the PD supports, any of 10BASE-T, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, and 10GBASE-T.

Autoclass Whether or not the PD requests Autoclass (yes or no).

Class 8 extended power Whether or not the single-signature PD makes use of the option to exceed the Class 8 P_{Class_PD} limit.

Class 5 extended power Whether or not the dual-signature PD makes use of the option to exceed the Class 5 $P_{Class\_PD\text{-}2P}$ limit.

PD evaluation system indicates whether the PD is an evaluation system.

DLL capability indicates that the PD supports the Power via MDI TLV and Data Link Layer classification.

NOTE—Single-signature PDs with a Requested Class greater or equal than 4 and dual-signature PDs with a Requested Class greater or equal than 4 on either Mode are required to indicate the DLL capability. PD evaluation systems are exempt from DLL tests and may indicate not having DLL capability.

For a single-signature PD, the PD's Logo Class is determined to be the requested Class of the PD. For a dual-signature PD, the PD's Logo Class is determined by the equivalence Table in Section 2.3.

2.3 Dual-signature Class equivalence

Dual-signature PDs provide an independent requested Class on the two pairsets. The requested Class may be different for each pairset, resulting in a large number of possible permutations. Table 1 indicates what the PD's Logo Class will be based on the requested Class of both pairsets of the dual-signature PD.

The determination of the equivalent Logo Class is based on three criteria:

1. The total power of the equivalent Logo Class must be equal to or lower than the sum power of each pairset
2. Since a dual-signature PD requires 4-pair power for both Modes to be powered, the minimum equivalent Logo Class is 5
3. The resulting maximum current on each pairset may not exceed the maximum current of the equivalent Logo Class

Table 1: Dual-signature PD requested Class to Logo Class mapping

Requested Class Mode X	Requested Class Mode Y	Power Mode A|B (W)	Power Mode B|A (W)	Total Power (W)	PD Logo Class
1	1	3.84	3.84	7.68	5
1	2	3.84	6.49	10.33	5
1	3	3.84	13.00	16.84	5
1	4	3.84	25.50	29.34	6
1	5	3.84	35.60	39.44	8
2	2	6.49	6.49	12.98	5
2	3	6.49	13.00	19.49	5
2	4	6.49	25.50	31.99	6
2	5	6.49	35.60	42.09	8
3	3	13.00	13.00	26.00	5
3	4	13.00	25.50	38.50	6
3	5	13.00	35.60	48.60	8
4	4	25.50	25.50	51.00	6
4	5	25.50	35.60	61.10	8
5	5	35.60	35.60	71.20	8

2.4 PSE requirements for dual-signature PDs

Based on the PSE's Logo Class this test plan requires a PSE to be able to support dual-signature PD's with a PD Logo Class that is equal or lower than the PSE's Logo Class. Table 2 shows an overview of these requirements.

Table 2: PSE support requirements for dual-signature PDs

PSE Logo Class	PD Requested Class Mode A|B	PD Requested Class Mode B|A	PD Logo Class
1 – 4	Support for 4-pair power is not required		
5	3	3	5
6	4	4	6
7	4	4	6
8	5	5	8

3 Document conventions

This section explains the guiding principles used in this document. The tests that make up the test suites for the various Power over Ethernet devices are designed to align as closely as possible to IEEE Std 802.3bt™-2018.

Several test models are defined (see Section 6). A test model is an abstract representation of a physical device that may be used to perform the test. Each of the test models have a default behavior, which is described

with the model definition. For example, the SSPD model in it's default state behaves as if it were an actual PD. By modifying parameters in the model the individual tests are able to elicit a particular behavior from the DUT and determine if the DUT meets the tested requirement.

Common sets of behavior are also described. By having a single description of e.g. classification, the tests can simply refer to these and make use of defined measurement parameters. This reduces the chance for errors in the tests and makes them as compact as possible. Section 7 describes the classification template. This applies to both the PSE test suite, where this template allows the tests to refer to a large number of parameters when measuring the classification behavior of the PSE, as well as the PD test suite, where this template allows the test to perform a particular classification behavior in a very compact but well defined way. Similarly Section 6.1.4 defines a power up sequence for the PD test suites.

3.1 Test description

Two test suites are defined, for PSEs (Section 9) and for single-signature PDs (Section 11). Each of the tests maps to a single requirement in IEEE Std 802.3bt™-2018, these requirements are summarized in the standard in the so called PICS (Protocol Implementation Conformance Statement) tables.

The tests are written to the following generic format:

PICS The first sentence of each test identifies which requirement is being tested. The PICS number is listed (e.g. PD15), as well as which subclause in IEEE Std 802.3bt™-2018 contains the requirement.

Last modification Lists the date when a particular test was modified. If the test was not modified since the initial release of the test plan this will state "Initial version".

History of changes is a list of changes that have been made to the test. Each change to the test is described with the date at which the modification became effective.

Test applicable to defines for which device this test applies. This determination uses only the required information as listed in Section 2.

Test order execution is listed for tests that must be executed first or last, see Section 4.2.

Test setup describes the starting conditions for the test. In the majority of tests a particular test fixture (see Section 6) is used, possibly with some modifications to one or more of it's parameters.

Test procedure is a numbered list of instructions on how to perform the test. The instructions are to be executed one after the other.

Pass requirements is a condition, or list of conditions that must be met in order for the device to pass the test.

3.2 References to IEEE Std 802.3bt™-2018

This test plan is written for IEEE Std 802.3bt™-2018 "IEEE Standard for Ethernet Amendment 2: Physical Layer and Management Parameters for Power over Ethernet over 4 pairs". IEEE Std 802.3bt™-2018 is available from `https://standards.ieee.org/project/802_3bt.html`

Tests refer to parameters and values listed in IEEE Std 802.3bt™-2018. Named parameters are preceded by an arrow sign "⇨", which indicates this is a parameter defined in IEEE Std 802.3bt™-2018.

4 Test execution

Tests are only performed when the device meets the criteria listed for "Test applicable to:".

The test setup describes the initial conditions that must be created before the test begins. This often involves connected a model to the device under test and configuring the model in a certain way.

The test procedure is executed by performing the steps one by one as outlined. During the test there may be instructions to measure or record a parameter, which is then subsequently used in the pass requirements to determine if the device under test meets the particular requirement. A repeat instruction "↻ Repeat" is used to perform multiple iterations of a given test. Before performing the next iteration of a test (due to the repeat statement), the pass requirements must be evaluated. In case there are multiple repeat statements consecutively, the pass requirements must be evaluated only for the innermost repeat loop.

4.1 Instruction timing

Instructions in the test procedure that do not involve a physical change (for example: marking time, calculating a variable, going back to a certain step, repeat statements, ...) are executed instantaneously and do not consume time. This is of particular importance for tests that create a voltage or current waveform with specific timing requirements.

Instructions that cause a physical change (set a voltage or current, make a measurement, connect or disconnect something, wait statements,...) will either have timing limits specified (if this is of consequence to the test), or, when not specified, the execution time of the instruction is not relevant to the outcome of the test and is left up to to the test implementer.

4.2 Order of testing

The order in which the tests are executed is free, with the exception that some tests' pass requirement is that they are executed first and subsequent tests pass. These tests are listed below.

4.2.1 PSE tests to be executed first

None.

4.2.2 Single-signature PD tests to be executed first

- PD8

4.3 Accuracy requirements

This subsection lists the required accuracy of measurements and accuracy of set parameters in the testing. Unless specifically overridden in a particular test, the accuracy values listed in Table 3 apply.

When a measurement value is used in a test as part of the pass requirement, any uncertainty with regard to pass or fail should be resolved in favor of passing the test. For example, if a measured voltage value must be below 10 V, and the measured value is 10.08 V, this must be considered as a pass.

Table 3: Measurement accuracy

Type of measurement	Unit	Required accuracy
Voltage	V	±max(1%, 50 mV)
Current	A	±max(1%, 100 µA)
Resistance	Ω	±1%
Capacitance	F	±5%

When a certain parameter is to be set (e.g. a voltage applied, or a resistance set), the accuracy requirements in Table 4 apply, unless otherwise specified in a test. When a test uses a range to denote how a parameter must be set, the accuracy listed in Table 4 does not apply, and the effectively set value must lie within the range.

Table 4: Parameter setting accuracy

Set parameter	Unit	Required accuracy
Voltage	V	±0.5 V
Current	A	±10 mA
Resistance	Ω	±1%

4.4 Inter-test wait time

For the PD test suite, the tester waits at least 6 s between any two separate tests where the PD is exposed to a voltage greater than 30 V during the test and any subsequent test. This prevents erroneous measurements resulting from residual charge in the PD's bulk capacitor.

5 Power Interface

The Power Interface (PI) is a term also used in IEEE Std 802.3bt™-2018 and is defined therein as "The mechanical and electrical interface between the Power Sourcing Equipment (PSE) or Powered Device (PD) and the transmission medium". All of the standards specifications apply at the PI. The tests defined in this test plan aim to make measurements as close to the PI as practically possible, or use compensation mechanisms where it is not possible.

The tests defined in this document use the PSE and PD PI naming convention defined in Figure 1. In the majority of the tests, voltages or currents are applied to a particular pair (eg. pair 1), which means that conductor 1 and conductor 2 are connected to each other and to the same potential.

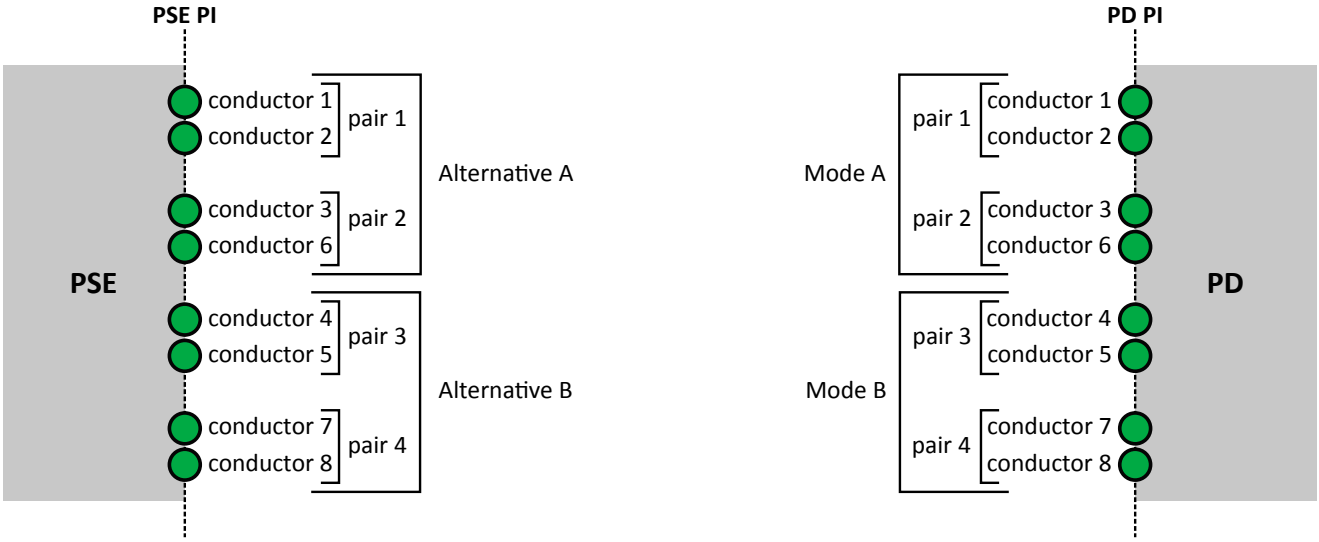

Figure 1: PSE and PD PI naming convention

The voltages at the PSE PI and PD PI are defined in Table 5. The Device Under Test (DUT), either a PSE or PD, will be connected to a test fixture. Note that there is a defined polarity for these; positive voltages match with the polarity configuration for Type 4 PSEs.

Additionally, the voltages V_{PSEPI} and V_{PDPI} are defined as:

$$V_{PSEPI} = \max\left(\left|V_{PSEPI\_A}\right|, \left|V_{PSEPI\_B}\right|\right)$$
$$V_{PDPI} = \max\left(\left|V_{PDPI\_A}\right|, \left|V_{PDPI\_B}\right|\right)$$

Table 5: PI voltage definitions

Parameter	Positive pair	Negative pair	Location
V_{PSEPI_A}	Pair 2	Pair 1	PSE PI (DUT)
V_{PSEPI_B}	Pair 3	Pair 4	PSE PI (DUT)
V_{PDPI_A}	Pair 2	Pair 1	PD PI (DUT)
V_{PDPI_B}	Pair 3	Pair 4	PD PI (DUT)

5.1 Connection between DUT PI and test fixture

The connection between the DUT and the test fixture is made using generic CAT5e category cable or better. The resistance of the pairs of the cable (two conductors in parallel) is defined as $R_{Cablepair n}$ in Figure 2. The test models defined in Section 6 are defined with an internal resistance on each pair, named $R_{PSEpair n}$ or $R_{PDpair n}$. These are in series with the cable resistances and together form $R_{pair n}$.

$$R_{pair n} = R_{Cablepair n} + R_{PDpair n}$$
$$R_{pair n} = R_{Cablepair n} + R_{PSEpair n}$$

Any length or gauge of cable may be used, provided that:

- The connection is straight through (DUT conductor 1 to test fixture conductor 1, DUT conductor 2 to test fixture conductor 2, ...)
- The total resistance of R_{pair1}, R_{pair2}, R_{pair3}, and R_{pair4} is less or equal to 6.25 Ω (unless more specific instructions are given in a particular test).
- The difference in resistance between the pairs (R_{pair1}, R_{pair2}, R_{pair3}, and R_{pair4}) meets the requirements in IEEE 802.3bt Clause 145A.3.

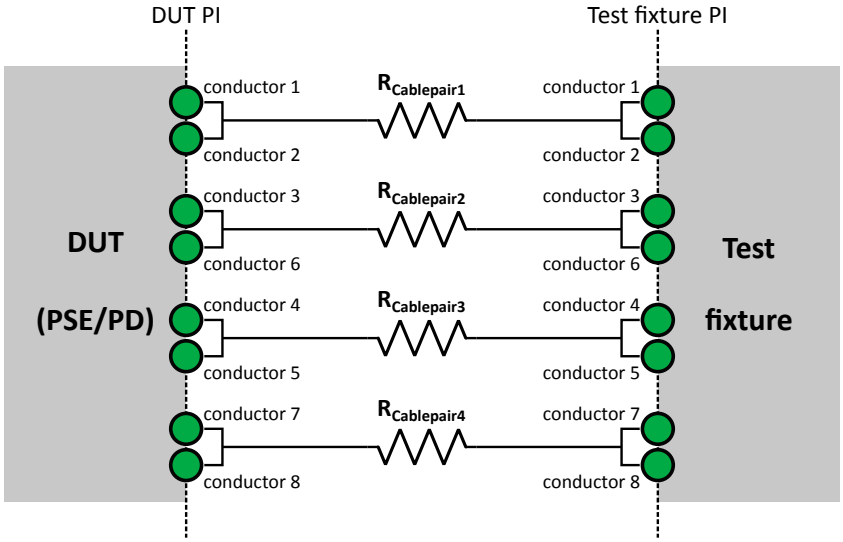

Figure 2: Default connection between a DUT and a test fixture

A test implementation may freely exchange resistance between $R_{Cablepair n}$ and $R_{PDpair n}$ or $R_{PSEpair n}$, so long that the value of $R_{pair n}$ meets the requirements above, or the more specific requirements of the test. This is done to provide freedom to implement the test.

The PSE and PD test fixtures include these cable resistances as part of the test fixture model. For the PSE model defined in Section 6.1, $R_{Cablepair n} = R_{PSEpair n}$, and for the PD models defined in Sections 6.2 and 6.3, $R_{Cablepair n} = R_{PDpair n}$.

5.1.1 Cable pair-to-pair unbalance

The requirements on the cable and connectors in IEEE Std 802.3bt™-2018 Annex 145A.3 define that the resistance unbalance between two pairs is:

$$\text{resistance unbalance} = \left\{ \left| \frac{R_{\text{Cablepair}x} - R_{\text{Cablepair}y}}{R_{\text{Cablepair}x} + R_{\text{Cablepair}y}} \right| \right\}_{\%} \quad (1)$$

Power over Ethernet devices are specified to work over cables and connectors that have a resistance unbalance smaller than 100 mΩ or less than 7% between the pairs (as defined in Equation 1), whichever is the greater unbalance.

In some tests the cable resistance is specifically set, for example the test would say "set (R_{pair1}, R_{pair2}, R_{pair3}, and R_{pair4}) in the range of 5 Ω to 6.25 Ω". For such a test it is permissible to use any value in the given range, however the pair resistances are still required to meet the resistance unbalance requirements.

6 Test fixtures

The test fixtures are abstract models that govern the behavior of actual test device implementations. These fixtures resemble usually either a PSE (when used to test PDs), or a PD (when used to test PSEs). The test fixtures however are not compliant PSEs or PDs. By the very nature of the test, these fixtures often need to show behavior disallowed by IEEE Std 802.3bt™-2018 in order to be able to test the DUT.

6.1 PSE model

The PSE model, defined in Figure 3, represents a PSE with two isolation switches. This model is used in the single-signature PD and dual-signature PD test suite.

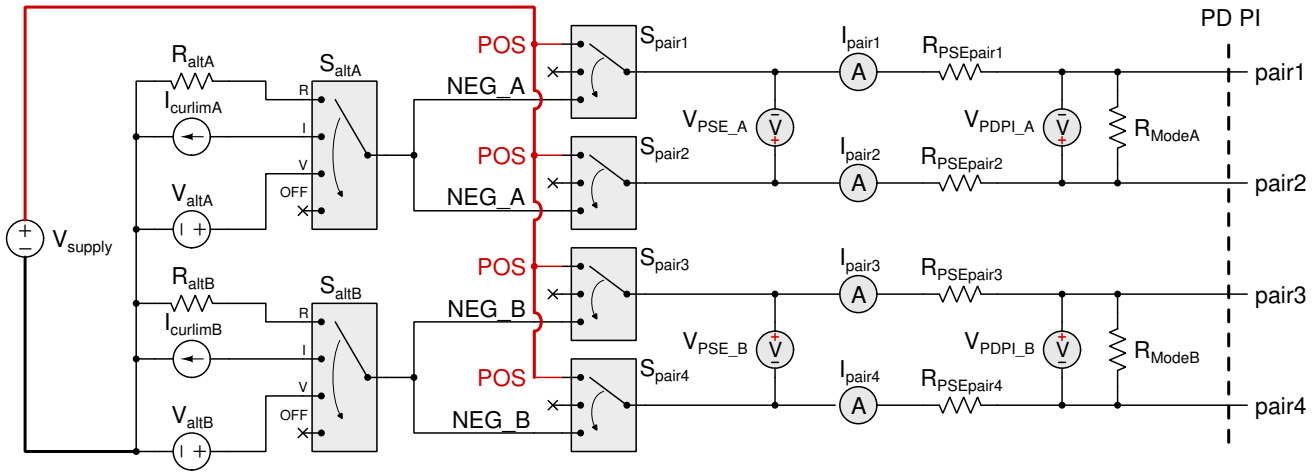

Figure 3: PSE model

6.1.1 PSE model elements

V_{supply} represents the common power supply for the test model. This supply will, depending on the specific test, be in the range of 50 V to 57 V [⇳$V_{Port\_PSE\text{-}2P}$].

S_{altA}, S_{altB} are switches that connect the negative pair of Alternative A and Alternative B to either a voltage sink (V_{altA} and V_{altB}), a current limiter ($I_{curlimA}$ and $I_{curlimB}$), or a resistance (R_{altA} and R_{altB}).

V_{altA}, V_{altB} are voltage sinks that oppose V_{supply}. These are used whenever a specific independent voltage is required on Alternative A or Alternative B. For example, if 10 V is to be applied to Mode B of a PD, then the test could state "Set V_{altB} such that $V_{PDPI\_B} = 10$ V." Assuming that $V_{supply} = 50$ V, V_{altB} would then be set to 40 V, resulting in the desired 10 V appearing at V_{PDPI_B}.

The voltage sinks are typically used when testing detection and classification and represent the voltage regulators found in PSE implementations that perform the same function. Even though this element is modeled as a "supply", it is only intended to force a specific voltage to appear at the PI, which will cause it to consume power.

$I_{curlimA}$, $I_{curlimB}$ are current limiters used to limit the current on the negative pairs independently. These are used during the inrush phase.

R_{altA}, R_{altB} are resistances in the negative pair that represent the PSE internal resistance while providing power.

S_{pair1}, S_{pair2}, S_{pair3}, S_{pair4} are switches that configure the PSE model PI. A pair can either be disconnected, connected to the positive supply rail, or connected to S_{altA} or S_{altB} for the negative pairs. With these switches any polarity configuration can be created, and also the number of powering pairs can be set.

V_{PSE_A}, V_{PSE_B} is the voltage for Alternative A and Alternative B, measured on the model side of the cable resistances $R_{PSEpair}n$.

I_{pair1}, I_{pair2}, I_{pair3}, I_{pair4} is the current through each of the four numbered pairs (see Section 5).

NOTE—All currents are positive, both for the negative pairs as for the positive pairs.

$R_{PSEpair1}$, $R_{PSEpair2}$, $R_{PSEpair3}$, $R_{PSEpair4}$ is the resistance between the DUT PI and the PSE test model.

NOTE—It is possible that these resistances are built into the test model implementation.

V_{PDPI_A}, V_{PDPI_B} is the voltage at the PD PI (DUT) for Mode A and for Mode B.

R_{ModeA}, R_{ModeB} is a resistance placed across a Mode.

6.1.2 Ethernet capability

The PSE model is required to support an Ethernet link with at least the following capabilities:

- Autonegotiation as specified in Clause 28 of IEEE Std 802.3™-2018
- 10BASE-T (full and half-duplex) as specified in Clause 14 of IEEE Std 802.3™-2018
- 100BASE-TX (full and half-duplex) as specified in Clause 25 of IEEE Std 802.3™-2018
- 1000BASE-T (full duplex) as specified in Clause 40 of IEEE Std 802.3™-2018
- 2.5GBASE-T (full duplex) as specified in Clause 126 of IEEE Std 802.3™-2018, only required if the PD to be tested indicates support for 2.5GBASE-T as specified in Section 2
- 5GBASE (full duplex) as specified in Clause 126 of IEEE Std 802.3™-2018, only required if the PD to be tested indicates support for 5GBASE-T as specified in Section 2
- 10GBASE-T (full duplex) as specified in Clause 55 of IEEE Std 802.3™-2018, only required if the PD to be tested indicates support for 10GBASE-T as specified in Section 2
- Energy Efficient Ethernet (if supported by the test fixture) **disabled**

6.1.3 Default parameter values

The default values for the PSE model are defined in Table 6. These are the values used unless specified differently in a particular test.

Table 6: Default values for the PSE model

Parameter	Note	Min	Max	Unit
V_{supply}	Supply voltage	52	56	V
	Supply current limit	3	5	A
V_{altA}, V_{altB}	Voltage	0	56	V
	Current sinking	—	—	A
	Current sourcing	—	0.015	A
R_{alt_A}, R_{alt_B}	"On" resistance negative pair	0.1	0.3	Ω
I_{curlim_A}, I_{curlim_B}	Current limiter	0.8	3	A
S_{altA}, S_{altB}	Switch between operation modes	OFF position		
$R_{PSEpair\,n}$	PSE model to DUT resistance, see 5.1.1 for unbalance	5	6.25	Ω
R_{ModeA}, R_{ModeB}	Resistance over a Mode	1	—	MΩ

6.1.4 Behavior

The initial state at the beginning of each test is as follows:

- S_{altA} and S_{altB} are in the "OFF" position
- S_{pair1}, S_{pair2}, S_{pair3}, and S_{pair4} are in the "X" position. If a test declares a particular power configuration in it's test setup this takes precedence.

When a test calls out to wait for the PD to be "powered up", this refers to at least 100 ms after $t_{classification\_end}$, as defined in Section 7.1. This ensures that the inrush phase of the PSE model is completed.

When a test refers to "power is removed" this refers to the voltage V_{PSEPI} being less than 2.8V for at least 15ms when the SSPD model is connected, and to V_{PSEPI_A} or V_{PSEPI_B} being less than 2.8V for at least 15ms for the called out pairset when the DSPD model is connected.

When a test in the PD test suite calls out to "apply an inrush and power on waveform" this refers to the following procedure:

1. V_{supply} is set in the ⇩$V_{Port\_PSE\text{-}2P}$ range (unless otherwise set by the test).
2. Set S_{altA} and/or S_{altB} to the "I" position in order to limit the current.
3. $I_{curlimA}$ and/or $I_{curlimB}$ is set to a value between 400 mA and 1.5 A. Let t_0 be the moment where the current limiter is set.
4. Wait an amount of time between 50 ms to 75 ms [⇩T_{Inrush}].
5. Set S_{altA} and/or S_{altB} to the "R" position.

The tests determine on which Alternative the inrush and power on waveform is to be applied.

Several tests require measurements of the current on the negative pairs. To determine the input average power, both the negative pair currents and the positive pair currents are required. For the PSE model, the following currents are defined:

$I_{pair\_negative\_A}$ is the current I_{pair1} or I_{pair2}, of whichever pair is at the negative potential of pair1 and pair2.

$I_{pair\_negative\_B}$ is the current I_{pair3} or I_{pair4}, of whichever pair is at the negative potential of pair3 and pair4.

$I_{pair\_negative}$ is the total current on the negative pairs: $I_{pair\_negative\_A} + I_{pair\_negative\_B}$.

$I_{pair\_positive\_A}$ is the current I_{pair1} or I_{pair2}, of whichever pair is at the positive potential of pair1 and pair2.

$I_{pair\_positive\_B}$ is the current I_{pair3} or I_{pair4}, of whichever pair is at the positive potential of pair3 and pair4.

$I_{pair\_positive}$ is the total current on the positive pairs: $I_{pair\_positive\_A} + I_{pair\_positive\_B}$.

6.1.5 Powering configurations

The valid PD powering configurations are defined in Table 7.

Table 7: Valid powering configurations for PDs

Pairsets	Mode A		Mode B	
Pairs Conductor	Pair 1 1 and 2	Pair 2 3 and 6	Pair 3 4 and 5	Pair 4 7 and 8
	Valid 2-pair connection			
PD_PCFG2–1	POS	NEG_A	—	—
PD_PCFG2–2	NEG_A	POS	—	—
PD_PCFG2–3	—	—	POS	NEG_B
PD_PCFG2–4	—	—	NEG_B	POS
	Valid 3-pair connection			
PD_PCFG3–1	POS	NEG_A	POS	—
PD_PCFG3–2	POS	NEG_A	—	POS
PD_PCFG3–3	NEG_A	POS	POS	—
PD_PCFG3–4	NEG_A	POS	—	POS
PD_PCFG3–5	POS	—	POS	NEG_B
PD_PCFG3–6	—	POS	POS	NEG_B
PD_PCFG3–7	POS	—	NEG_B	POS
PD_PCFG3–8	—	POS	NEG_B	POS
	Valid 4-pair connection			
PD_PCFG4–1	NEG_A	POS	NEG_B	POS
PD_PCFG4–2	NEG_A	POS	POS	NEG_B
PD_PCFG4–3	POS	NEG_A	NEG_B	POS
PD_PCFG4–4	POS	NEG_A	POS	NEG_B

POS denotes a pair connected to the positive supply voltage of the source
NEG_A denotes a pair connected to the negative supply voltage of the source on pair 1 or pair 2
NEG_B denotes a pair connected to the negative supply voltage of the source on pair 3 or pair 4
— denotes a pair not connected to the supply voltage (open connection)

6.1.6 Calculation of highest average power

An average power measurement of a PD may be calculated for the whole device or on a per Mode basis, and is based on a 1 second interval. The calculation of the highest average power is based on a sliding window with a width of 1 second and at least 10 instant power measurements per second. Unless specified differently, a highest average power is determined over at least 5 s.

Average power when operating in the PD_PCFG2–1 or PD_PCFG2–2 configuration or average power for Mode A only is calculated as follows:

$$\text{highest average power} = \max\left\{\int_{t}^{t+1\,\text{s}} I_{\text{pair\_negative\_A}} \times V_{\text{PDPI\_A}}\, dt : t = t_{\text{start}} \cdots t_{\text{end}}\right\} \tag{2}$$

Average power when operating in the PD_PCFG2–3 or PD_PCFG2–4 configuration or average power for Mode B only is calculated as follows:

$$\text{highest average power} = \max\left\{\int_{t}^{t+1\,\text{s}} I_{\text{pair\_negative\_B}} \times V_{\text{PDPI\_B}}\, dt : t = t_{\text{start}} \cdots t_{\text{end}}\right\} \tag{3}$$

Average power when operating in any of the PD_PCFG3 or PD_PCFG4 configurations requires the measured voltages as listed in Table 8.

Table 8: Power measurement required voltage measurements

$\lvert V_{\text{PDPI\_A}}\rvert$	The absolute voltage between pair1 and pair2 at the PD PI.
$\lvert V_{\text{PDPI\_B}}\rvert$	The absolute voltage between pair3 and pair4 at the PD PI.
$V_{\text{PDPI\_}\Delta\text{pos}}$	The voltage between the positive pair of Mode A (pair1 or pair2) and the positive pair of Mode B (pair3 or pair4). The positive terminal of the meter is to be connected to the Mode A positive pair.
$V_{\text{PDPI\_}\Delta\text{neg}}$	The voltage between the negative pair of Mode A (pair1 or pair2) and the negative pair of Mode B (pair3 or pair4). The positive terminal of the meter is to be connected to the Mode A negative pair.

And the highest average power itself is defined as:

$$\max\left\{\int_{t}^{t+1\,\text{s}} I_{\text{pair\_negative}} \cdot \left(V_{\text{PDPI\_A}} - \frac{I_{\text{pair\_positive\_B}}}{I_{\text{pair\_negative}}} \cdot V_{\text{PDPI\_}\Delta\text{pos}} - \frac{I_{\text{pair\_negative\_A}}}{I_{\text{pair\_negative}}} \cdot V_{\text{PDPI\_}\Delta\text{neg}}\right) dt : t = t_{\text{start}} \cdots t_{\text{end}}\right\} \tag{4}$$

6.2 Single-signature PD model

The SSPD model, defined in Figure 4, represents a single-signature PD. This model is used in the PSE test suite.

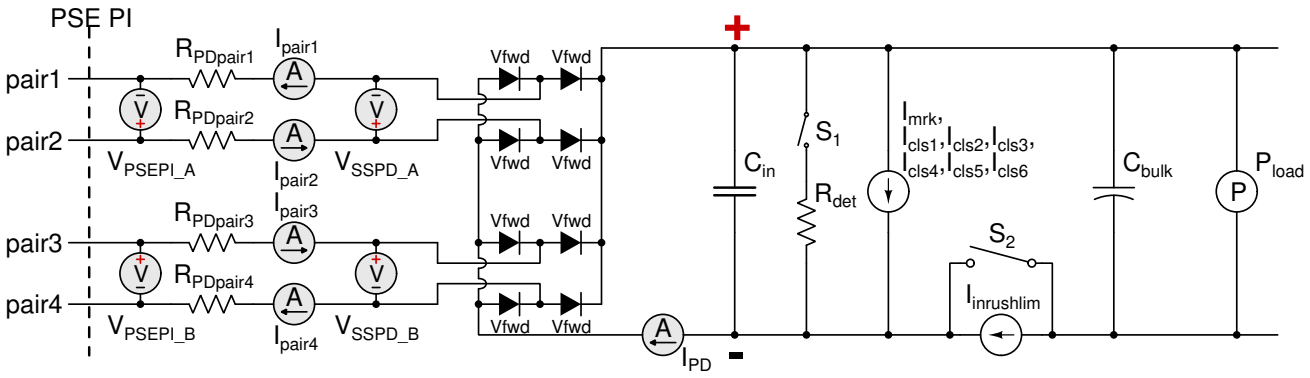

Figure 4: Single-signature PD model (SSPD)

6.2.1 Single-signature PD model elements

V_{PSEPI_A}, V_{PSEPI_B} are the voltages on Alternative A and Alternative B at the PSE (DUT) PI.

$R_{PDpair1}$, $R_{PDpair2}$, $R_{PDpair3}$, $R_{PDpair4}$ is the resistance between the DUT PI and the PD test model.

NOTE—It is possible that these resistances are built into the test model implementation.

I_{pair1}, I_{pair2}, I_{pair3}, I_{pair4} is the current through each of the four numbered pairs (see Section 5).

V_{SSPD_A}, V_{SSPD_B} is the voltage for Mode A and Mode B, measured on the model side of the cable resistances $R_{PDpairn}$.

V_{fwd} represents the forward voltage per pair of the rectifier in the SSPD model.

I_{PD} is the total current drawn by the SSPD model.

C_{in} is the capacitance before the isolation switch (S2).

R_{det} is the detection resistance.

S_1 is a switch for R_{det}.

I_{mrk} is a current sink to draw mark currents.

I_{cls1} through I_{cls6} are current sinks to draw currents during the various class events.

S_2 is the isolation switch for the load side of the SSPD model (C_{bulk} and ⇨P_{load}).

$I_{inrushlim}$ is a current limiter used to control the current during inrush.

C_{bulk} is a capacitor on the load side of the isolation switch.

⇨P_{load} is a constant power load.

6.2.2 Default parameter values

The default values for the SSPD model are defined in Table 9 and Table 10. These are the values used unless specified differently in a particular test.

Table 9: Default values for SSPD (not based on assigned Class)

Parameter	Description	Min	Max	Unit
pd_req_class	PD requested Class	1	8	—
$R_{PDpair n}$	DUT to model resistance, see 5.1.1	5	6.25	Ω
V_{fwd}	PD voltage offset	0	0.95	V
C_{in}	PD capacitance when the PD is “off”	50	120	nF
R_{det}	PD detection resistance	23.7	26.3	kΩ
I_{mrk}	Mark current	0.25	4	mA
$I_{inrushlim}$	PD inrush current (self limited case)	50	380	mA
C_{bulk}	PD additional capacitance when “on”	10	180	µF
P_{load}	PD constant input power ($V_{SSPD} \times I_{PD}$)	2	3.5	W
sspd_autoclass	Physical Layer Autoclass		FALSE	

Table 10: Class currents based on requested Class for the SSPD model in Figure 4

Parameter	PD Class	Description	Min	Max	Unit
I_{cls1}, I_{cls2}	0	class events EV1 and EV2	0	5	mA
	1	class events EV1 and EV2	8	13	mA
	2	class events EV1 and EV2	16	21	mA
	3	class events EV1 and EV2	25	31	mA
	4	class events EV1 and EV2	35	45	mA
	5	class events EV1 and EV2	35	45	mA
	6	class events EV1 and EV2	35	45	mA
	7	class events EV1 and EV2	35	45	mA
	8	class events EV1 and EV2	35	45	mA
I_{cls3}, I_{cls4},	0	class events EV3 through EV6	0	5	mA
I_{cls5}, I_{cls6}	1	class events EV3 through EV6	8	13	mA
	2	class events EV3 through EV6	16	21	mA
	3	class events EV3 through EV6	25	31	mA
	4	class events EV3 through EV6	35	45	mA
	5	class events EV3 through EV6	0	5	mA
	6	class events EV3 through EV6	8	13	mA
	7	class events EV3 through EV6	16	21	mA
	8	class events EV3 through EV6	25	31	mA

6.2.3 Behavior

The behavior of the SSPD model is defined by the “Single-signature PD state diagram” in Figure 145–25 of IEEE Std 802.3bt™-2018. The mapping between state diagram variables and behavior elements in the SSPD

Table 11: State diagram to SSPD behavior mapping

State diagram variable			SSPD model element
⇨V_{PD}		⇐	V_{SSPD}
pd_autoclass_enable		⇐	sspd_autoclass
present_class_sig_0			
	FALSE	⇒	—
	TRUE	⇒	I_{cls1} = 0 mA to 4 mA
present_class_sig_A			
	FALSE	⇒	I_{cls1}, I_{cls2} = 0 mA
	TRUE	⇒	I_{cls1}, I_{cls2} = set per Table 10
present_class_sig_B			
	FALSE	⇒	I_{cls3}, I_{cls4}, I_{cls5}, I_{cls6} = 0 mA
	TRUE	⇒	I_{cls3}, I_{cls4}, I_{cls5}, I_{cls6} = set per Table 10
present_det_sig			
	either	⇒	S_1 = open or closed
	invalid	⇒	S_1 = open
	valid	⇒	S_1 = closed
present_mark_sig			
	FALSE	⇒	I_{cls3}, I_{cls4}, I_{cls5}, I_{cls6} = 0 mA
	TRUE	⇒	I_{cls3}, I_{cls4}, I_{cls5}, I_{cls6} = set per Table 10
pd_max_power			
	0	⇒	S_2 = open, $I_{inrushlim}$ = 0 mA
	inrush	⇒	S_2 = open, $I_{inrushlim}$ = set per Table 9
	1 through 8	⇒	S_2 = closed, $I_{inrushlim}$ = 0 mA

model are defined in Table 11.

The internal voltage V_{SSPD} is defined as:

$$V_{SSPD} = \max\left(\left|V_{SSPD\_A}\right|, \left|V_{SSPD\_B}\right|\right)$$

Several tests require measurements of the current on the negative pairs, because several requirements apply to negative pair current only. For the SSPD model, the following currents are defined:

I_{PDA} is the current I_{pair1} or I_{pair2}, of whichever pair is at the negative potential of pair1 and pair2.

I_{PDB} is the current I_{pair3} or I_{pair4}, of whichever pair is at the negative potential of pair3 and pair4.

6.2.4 DUT PI voltage measurements

The voltage measurements V_{PSEPI_A} and V_{PSEPI_B} represent the voltages at the DUT PSE PI. Given that the SSPD model is connected to the DUT using a cable, with pair resistances ($R_{Cablepair\,n}$) as defined in Section 5.1, note that measurements need to be corrected for any voltage drop incurred by $R_{Cablepair\,n}$, such that measurements meet the uncertainty requirements prescribed by Section 4.3.

6.2.5 Offset voltage

The offset voltage of the SSPD model (V_{fwd}) is related to ⇩V_{offset} in IEEE Std 802.3bt™-2018. It represents the forward voltage drop of any series diodes used in the rectification stage. Measured between a pairset, two such voltage drops may occur, resulting in both specifications being the same.

6.2.6 P_{load} power tolerance

When P_{load} is set to a value P for a particular test, the actual drawn power may be in the range of $(P-1\,W)$ to P, except where a different power tolerance is given in a particular test.

6.2.7 Reflected voltage

The requirement on the SSPD's reflected behavior differs from that in IEEE Std 802.3bt™-2018. When the SSPD is connected through any of the valid 2-pair, or any of the valid 3-pair connections, at any supply voltage, the reflected voltage on the Mode with at least one open connection, shall be less than 2.8 V with any resistance of 0 kΩ to 100 kΩ attached to said Mode.

This tighter requirement is needed in order to be able to measure if a PSE is providing 4-pair power or not.

6.2.8 Pair to pair current unbalance

The SSPD model is required to meet the same pair to pair current unbalance requirements that a single-signature PD must meet. Specifically, the SSPD model is required to pass the PD unbalance tests defined in 11.68 and 11.69.

6.3 Dual-signature PD model

The DSPD model, defined in Figure 5, represents a dual-signature PD. This model is used in the PSE tests.

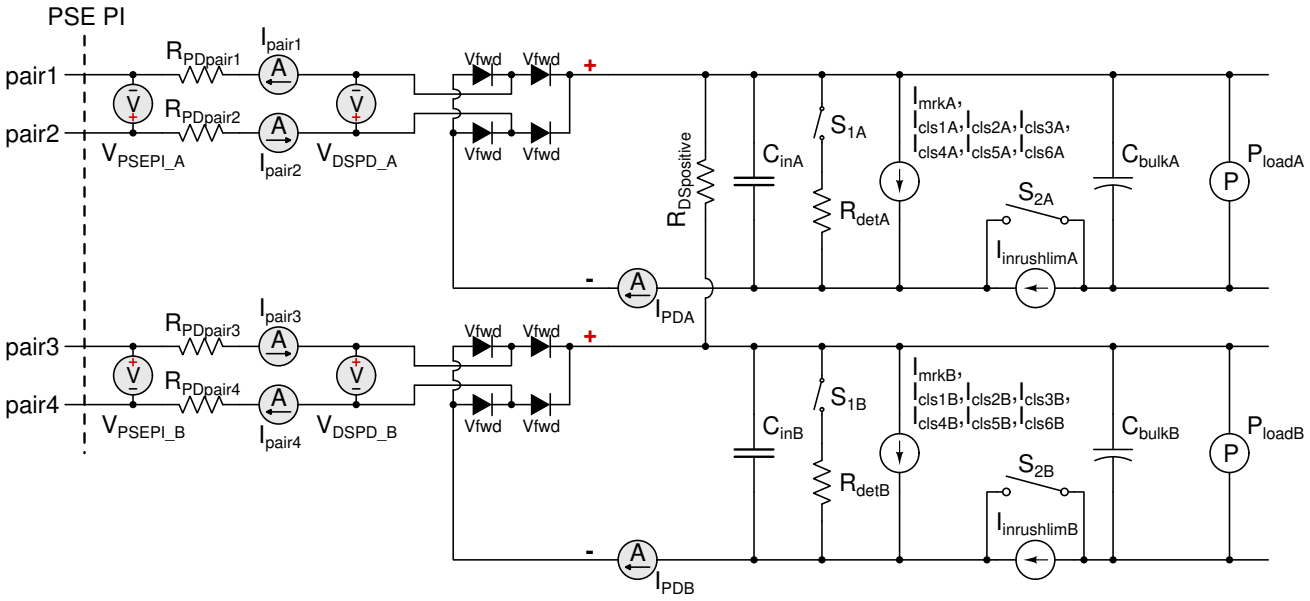

Figure 5: Dual-signature PD model (DSPD)

6.3.1 Dual-signature PD model elements

V_{PSEPI_A}, V_{PSEPI_B} are the voltages on Alternative A and Alternative B at the PSE (DUT) PI.

$R_{PDpair1}$, $R_{PDpair2}$, $R_{PDpair3}$, $R_{PDpair4}$ is the resistance between the DUT PI and the PD test model.

NOTE—It is possible that these resistances are built into the test model implementation.

I_{pair1}, I_{pair2}, I_{pair3}, I_{pair4} is the current through each of the four numbered pairs (see Section 5).

V_{DSPD_A}, V_{DSPD_B} is the voltage for Mode A and Mode B, measured on the model side of the cable resistances $R_{PDpairn}$.

V_{fwd} represents the forward voltage per pair of the rectifier in the SSPD model.

I_{PDA}, I_{PDB} is the total current drawn by the SSPD model on the negative pair of Mode A and Mode B respectively.

$R_{DSpositive}$ is the resistance between the positive rails of Mode A and Mode B.

C_{inA}, C_{inB} is the capacitance before the isolation switch (S2) of Mode A and Mode B respectively.

R_{detA}, R_{detB} is the detection resistance of Mode A and Mode B respectively.

S_{1A}, S_{1B} are switches for R_{detA} and R_{detB} respectively.

I_{mrkA}, I_{mrkB} are current sinks to draw mark currents for Mode A and Mode B respectively.

I_{cls1A} through I_{cls6A}, I_{cls1B} through I_{cls6B} are current sinks to draw currents during the various class events for Mode A and Mode B respectively.

S_{2A}, S_{2B} are the isolation switches for the load side of the DSPD model on Mode A and Mode B respectively.

$I_{inrushlimA}$, $I_{inrushlimB}$ are current limiters used to control the current during inrush.

C_{bulkA}, C_{bulkB} are capacitors on the load side of the isolation switch on Mode A and Mode B respectively.

P_{loadA}, P_{loadB} are constant power loads for Mode A and Mode B respectively.

6.3.2 Default parameter values

The default values for the DSPD model are defined in Table 12 and Table 13. These are the values used unless specified differently in a particular test.

Table 12: Default values for DSPD (not based on assigned Class)

Parameter	Description	Min	Max	Unit
pd_req_class_mode (A/B)	PD requested Class	1	5	—
$R_{PDpair\,n}$	DUT to model resistance, see 5.1.1	5	6.25	Ω
V_{fwd}	PD voltage offset	0	0.95	V
$R_{DSpositive}$	Resistance between positive pairs	1000	—	kΩ
C_{inA}, C_{inB}	PD capacitance when the PD is “off”	50	120	nF
R_{detA}, R_{detB}	PD detection resistance	23.7	26.3	kΩ
I_{mrkA}, I_{mrkB}	Mark current	0.25	4	mA
$I_{inrushlimA}$, $I_{inrushlimB}$	PD inrush current (self limited case)	50	380	mA
C_{bulkA}, C_{bulkB}	PD additional capacitance when “on”	10	180	µF
P_{load_delayA}, P_{load_delayB}	PD wait time before full power	80	—	ms
P_{loadA}, P_{loadB}	PD constant input power ($V_{DSPD\_A} \times I_{PDA}$, $V_{DSPD\_B} \times I_{PDB}$)	2	3.5	W

Table 13: Class currents based on requested Class for the DSPD model in Figure 4

Parameter	PD Class	Description	Min	Max	Unit
I_{cls1A}, I_{cls1B},	1	class events EV1 and EV2	8	13	mA
I_{cls2A}, I_{cls2B}	2	class events EV1 and EV2	16	21	mA
	3	class events EV1 and EV2	25	31	mA
	4	class events EV1 and EV2	35	45	mA
	5	class events EV1 and EV2	35	45	mA
I_{cls3A}, I_{cls3B},	1	class events EV3 through EV5	0	5	mA
I_{cls4A}, I_{cls4B},	2	class events EV3 through EV5	0	5	mA
I_{cls5A}, I_{cls5B},	3	class events EV3 through EV5	0	5	mA
	4	class events EV3 through EV5	0	5	mA
	5	class events EV3 through EV5	25	31	mA

Table 14: State diagram to DSPD behavior mapping

State diagram variable			DSPD model element
$\eth V_{PD}$_mode(X)		$\Leftarrow$	V_{SSPD_x}
present_class_sig_A_mode(X)			
	FALSE	$\Rightarrow$	I_{cls1x}, $I_{cls2x} = 0$ mA
	TRUE	$\Rightarrow$	I_{cls1x}, I_{cls2x} = set per Table 10
present_class_sig_B_mode(X)			
	FALSE	$\Rightarrow$	I_{cls3x}, I_{cls4x}, I_{cls5x}, $I_{cls6x} = 0$ mA
	TRUE	$\Rightarrow$	I_{cls3x}, I_{cls4x}, I_{cls5x}, I_{cls6x} = set per Table 10
present_det_sig_mode(X)			
	either	$\Rightarrow$	S_{1x} = open or closed
	invalid	$\Rightarrow$	S_{1x} = open
	valid	$\Rightarrow$	S_{1x} = closed
present_mark_sig_mode(X)			
	FALSE	$\Rightarrow$	I_{cls3x}, I_{cls4x}, I_{cls5x}, $I_{cls6x} = 0$ mA
	TRUE	$\Rightarrow$	I_{cls3x}, I_{cls4x}, I_{cls5x}, I_{cls6x} = set per Table 10
pd_max_power_mode(X)			
	0	$\Rightarrow$	S_{2x} = open, $I_{inrushlim} = 0$ mA
	inrush	$\Rightarrow$	S_{2x} = open, $I_{inrushlim}$ = set per Table 9
	1 through 8	$\Rightarrow$	S_{2x} = closed, $I_{inrushlim} = 0$ mA

6.3.3 Behavior

The behavior of the DSPD model is defined by the "Dual-signature PD state diagram" in Figure 145–27 of IEEE Std 802.3bt™-2018. The mappings between state diagram variables and behavior elements in the DSPD model are defined in Table 14.

Note that the behavior for Mode A and Mode B is independent and is noted in this Table using the notation *X* where *X* can refer to "A" for Mode A and "B" for Mode B.

6.3.4 DUT PI voltage measurements

The voltage measurements V_{PSEPI_A} and V_{PSEPI_B} represent the voltages at the DUT PSE PI. Given that the DSPD model is connected to the DUT using a cable, with pair resistances ($R_{Cablepair\,n}$) as defined in Section 5.1, note that measurements need to be corrected for any voltage drop incurred by $R_{Cablepair\,n}$, such that measurements meet the uncertainty requirements prescribed by Section 4.3.

6.3.5 Offset voltage

The offset voltage of the DSPD model is related to $\eth V_{offset}$ in IEEE Std 802.3bt™-2018. It represents the forward voltage drop of any series diodes used in the rectification stage. Measured between a pairset, two such voltage drops may occurs, resulting in both specifications being the same.

6.3.6 P_{loadA} and P_{loadB} power tolerance

When P_{loadA} or P_{loadB} is set to a value P for a particular test, the actual drawn power may be in the range of $(P-1\,W)$ to P, except where a different power tolerance is given in a particular test.

6.3.7 Reflected voltage

When the DSPD is connected through any of the valid 2-pair, or any of the valid 3-pair connections, at any supply voltage, the backfeed voltage on the Mode with at least one open connection, shall be less than 2.8 V with any resistance of 0 kΩ to 100 kΩ attached to said Mode.

7 Classification template

Classification is the process whereby the PSE learns about the PD's requested Class, and simultaneously the PSE informs the PD about the assigned Class. The generic classification voltage waveform and corresponding parameters are listed in Figure 6.

This figure and these parameters are used in both the PSE and PD test suite. In the PSE test suite the waveform is generated by the PSE Device Under Test (DUT), and the tests will make references to measurement parameters. In the PD test suite these parameters will be set in order to generate a specific waveform to test the PD DUT.

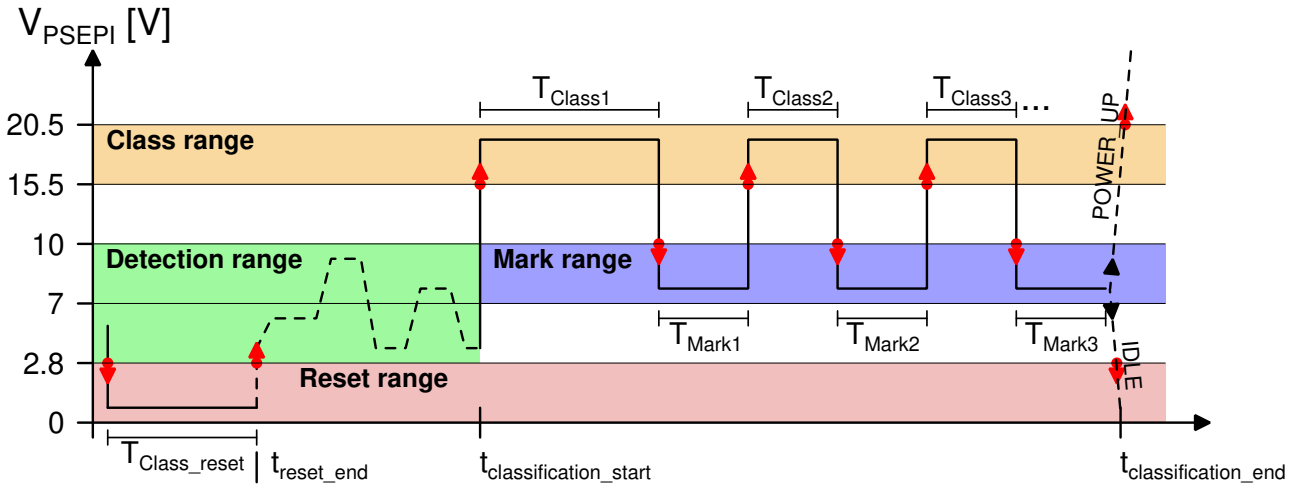

Figure 6: Classification waveform, reference points, and parameters

7.1 Parameter description

This subsection provides a short description of all of the named elements and parameters that are used in classification. Figure 6 provides a schematic overview of a classification waveform and Table 15 lists the default values for these parameters.

Class range is the voltage range the PSE produces to generate a class event.

Detection range is the voltage range the PSE can use to perform detection and connection check. The specific waveforms inside this range are not specified in the standard. We no longer refer to the detection range once the voltage has been in the Class range, until the voltage has been in the reset range for at least 15 ms.

Mark range is the voltage range the PSE produces to generate a mark event. The mark even denotes the end of a class event. The mark range overlaps completely with a part of the detection range.

Reset range is the voltage range the PSE produces when in one of the IDLE or ERROR states, or when it is resetting the PD's class event count.

$\mathbf{t_{reset\_end}}$ is the moment in time where the voltage enters the detection range from the reset range.

$\mathbf{t_{reset\_end}}$ is only marked after the voltage has been in the reset range for at least 15 ms.

$t_{classification\_start}$ is the moment in time where the voltage enters the class range for the first time after a reset.

$t_{classification\_startA}$ is the moment in time where the voltage enters the class range for the first time after a reset on Alternative A or Mode A.

$t_{classification\_startB}$ is the moment in time where the voltage enters the class range for the first time after a reset on Alternative B or Mode B.

$t_{classification\_end}$ is the moment in time where the voltage exceeds the maximum value of the class range for the first time after a reset.

$t_{classification\_endA}$ is the moment in time where the voltage exceeds the maximum value of the class range for the first time after a reset on Alternative A or Mode A.

$t_{classification\_endB}$ is the moment in time where the voltage exceeds the maximum value of the class range for the first time after a reset on Alternative B or Mode B.

T_{Class_reset} is the measured or set time duration where the voltage is continuously in the reset range.

$T_{Class}n$ is the measured or set time duration where the voltage is in the class range for the n^{th} class event.

$I_{Class}n$ is the measured current on all negative pairs during the n^{th} class event.

$I_{Class}n\_A$ is the measured current on the negative pair of Alternative A during the n^{th} class event.

$I_{Class}n\_B$ is the measured current on the negative pair of Alternative B during the n^{th} class event.

$T_{Mark}n$ is the measured or set time duration where the voltage is in the mark range for the n^{th} mark event.

$I_{Mark}n$ is the measured current on all negative pairs during the n^{th} mark event.

$I_{Mark}nA$ is the measured current on the negative pair of Alternative A during the n^{th} mark event.

$I_{Mark}nB$ is the measured current on the negative pair of Alternative B during the n^{th} mark event.

class_event_count is the number of classification events counted or generated.

sspd_autoclass is a variable that can be set TRUE or FALSE and indicates if the SSPD model requests Physical Layer Autoclass during the first class event.

pd_requested_class is the determined PD requested Class for a single-signature PD (see 7.3.3).

pd_requested_classA is the determined PD requested Class for Mode A of a dual-signature PD.

pd_requested_classB is the determined PD requested Class for Mode B of a dual-signature PD.

pse_assigned_class is the assigned Class for a single-signature PD (see 7.3.3).

pse_assigned_classA is the assigned Class for Mode A of a dual-signature PD.

pse_assigned_classB is the assigned Class for Mode A of a dual-signature PD.

7.2 PSE classification measurement

When a test in the PSE test suite calls out to "perform a classification waveform measurement", the parameters listed in Section 7.1 are measured. In addition the parameter class_event_count is calculated as follows:

- class_event_count is set to zero whenever the voltage has been in the reset range continuously for at least $\Rightarrow T_{Reset}$.
- class_event_count is incremented by one whenever the voltage has been in the class range continuously for at least 6 ms, followed by the voltage being in the mark event range continuously for at least 6 ms.

A "classification sequence" is defined as the time between $t_{classification\_start}$ and $t_{classification\_end}$ and consists of at least one postive transition into the class voltage range followed by a transition either to a power state (voltage exceed the class range) or a return to an idle state (voltage goes into the reset range for at least 15 ms).

When the connected test fixture is the SSPD model, the voltage measurement is based on V_{PSEPI}, and the current is the total current on the negative pairs (equivalent to I_{PD}). When the connected test fixture is the DSPD model, the classification waveform measurement is measure idependently for each pairset. The voltages are V_{PSEPI_A} and V_{PSEPI_B}, and the corresponding currents are I_{PDA} and I_{PDB}.

7.3 PD classification generation

When a test in the PD test suite calls out to "apply a classification waveform", the electrical and timing parameters listed in Table 15 apply, as well as the general waveform shown in Figure 6. Specific tests may override the default values in this Table.

The parameter class_event_count, when set in the test, determines the number of class and mark events that are produced, regardless of the requested Class of the PD. This allows a test to produce a waveform with a fixed number of classification events.

Alternatively, the test may set psemodel_max_class to perform classification per the classification rules outlined in Table 16 or Table 17, which follow the rules in IEEE Std 802.3bt™-2018. When this is set, psemodel_max_class is the equivalent of pse_avail_pwr in the PSE state diagram. Table 16 corresponds with the classification rules for single-signature PDs, where Table 17 corresponds with the classification rules for dual-signature PDs.

By default, if not specified in the test, the value of psemodel_max_class is set to 8, psemodel_max_classA and psemodel_max_classB are set to 5, and class_event_count is not set. The PSE model performs classification according to the normal rules outlined in Table 16 or Table 17.

When applying a classification waveform, the PSE model is permitted to create any waveforms in the detection range, provided these do not exceed 10 V. Note that the PSE model is not required to perform detection or connection check prior to apply class range voltage or operating power.

During a classification waveform the S_{altA} or S_{altB} switch is set to the "V" position to generate the required voltages. At the conclusion of a classification waveform the switch remains in the "V" position. The output voltage for V_{PSE_A} or V_{PSE_B} is in the 7 V to 10 V [$\Rightarrow V_{Mark}$] range.

7.3.1 Power configuration during classification

Depending on the power configuration selected in a test (see Table 7) and whether the PD is a single- or dual-signature device, the generated class and mark events must be output on Alternative A, Alternative B, or both.

For single-signature PDs, the class and mark events must be generated on Alternative A (using V_{altA}) when power configurations PD_PCFG2–1, PD_PCFG2–2, or PD_PCFG3–1 through PD_PCFG3–4 is selected. When PD_PCFG2–3, PD_PCFG2–4, or PD_PCFG3–5 through PD_PCFG3–8 is selected, the events must be generated on Alternative B (using V_{altB}). When operating in 4-pair mode, with configuration PD_PCFG4–x, the events may be generated on either Alternative, or on both Alternatives simultaneously. In the latter case, the PSE model must read both $I_{pair\_negative\_A}$ and $I_{pair\_negative\_B}$ to determine the return current.

For a dual-signature PD, the class and mark events are generated seperately for Alternative A and Alternative B. This choice must be indicated in the test. The classification waveforms for Alternative A and Alternative B may be generated sequentially or simultaneously.

7.3.2 Class signature measurement

In order to determine the class signature generated by the PD during the first two class events (class_sig_A) and during any subsequent events (class_sig_B), the PSE model measures the drawn current.

For the first class event, the measurement (or measurements) are performed within $t_{class\_measure\_LCE}$. For any subsequent class events, measurements are performed within $t_{class\_measure}$.

If the length of the first class event (T_{Class1}) is greater than or equal to 88 ms, a second measurement of the class current is performed at least 87.5 ms [$\Rightarrow T_{ACS}$ max] after the beginning of the class event and before the conclusion of the first class event. The resulting class signature is recorded as class_sig_auto. When I_{Class1} is any of class signatures 1, 2, 3, or 4, and class_sig_autocorresponds with class signature 0, this signifies that the PD is requesting Physical Layer Autoclass.

For a single-signature PD the total amount of current on the negative pairs determines the class signature. Table 15 maps the valid current ranges to the class signature. Current readings outside these ranges constitute an invalid class signature and cause failure of any test in which these are encountered.

Measurements of the Autoclass class signature are performed during the first class event within the time period $t_{class\_measure\_autoclass}$.

Table 15: Classification electrical and timing parameters

Parameter	Note	Min	Max	Unit
Class range voltage		15.5	20.5	V
Mark range voltage		7	10	V
Detection range voltage	Not applicable in classification	2.8	10	V
Reset range voltage		0	2.8	V
T_{Class_reset}		15	—	ms
T_{Class1}		88	—	ms
T_{Class2}		6	—	ms
T_{Class3}		6	—	ms
T_{Class4}		6	—	ms
T_{Class5}		6	—	ms
T_{Mark1}		88	—	ms
T_{Mark2}		6	—	ms
T_{Mark3}		6	—	ms
T_{Mark4}		6	—	ms
T_{Mark5}		6	—	ms
$t_{class\_measure\_LCE}$	referenced from beginning of first class event	5	75.5	ms
$t_{class\_measure}$	referenced from beginning of class event	5	end	ms
$t_{class\_measure\_autoclass}$	referenced from beginning of first class event	87.5	end	ms
Class signature 0		1	4	mA
Class signature 1		9	12	mA
Class signature 2		17	20	mA
Class signature 3		26	30	mA
Class signature 4		36	44	mA

“end” refers to the end of the class event

Table 16: Number of class events as result of the PD's requested Class and the value of psemodel_max_class (single-signature)

PD requested Class	class_sig_A	class_sig_B	psemodel_max_class	⇒	class_event_count
1	1	1	1 – 8		1
2	2	2	1		—
			2 – 8		1
3	3	3	1 – 2		—
			3 – 8		1
4	4	4	1 – 2		—
			3		1
			4 – 8		2, 3
5	4	0	1 – 2		—
			3		1
			4		2, 3
			5 – 8		4
6	4	1	1 – 2		—
			3		1
			4 – 5		2, 3
			6 – 8		4
7	4	2	1 – 2		—
			3		1
			4		2, 3
			6		4
			7 – 8		5
8	4	3	1 – 2		—
			3		1
			4		2, 3
			6 – 7		4
			8		5

— denotes that the PSE is unable to allocate the requested amount of power, and will not turn on.

Table 17: Number of class events as result of the PD's requested Class and the value of psemodel_max_class (dual-signature)

PD requested Class (Mode X)	class_sig_A	class_sig_B	psemodel_max_class*X*	⇒	class_event_count
1	1	0	1 – 5		1, 2, 3
2	2	0	1		—
			2 – 5		1, 2, 3
3	3	0	1 – 2		—
			3 – 5		1, 2, 3
4	4	0	1 – 2		—
			3		1
			4 – 5		2, 3
5	4	3	1 – 2		—
			3		1
			4		2, 3
			5		4

— denotes that the PSE is unable to allocate the requested amount of power, and will not turn on.

7.3.3 Determination of the PD requested Class and PSE assigned Class

Based on the class signatures generated by a PD and the number of class events generated by a PSE the assigned Class can be derived. For single-signature PDs, the assigned Class is referred to as "pse_assigned_class", for dual-signature PDs it is referred to as "pse_assigned_classA" and "pse_assigned_classB" for Mode A and Mode B respectively.

The number of class events that are generated by the PSE model is controlled by the parameters psemodel_max_class and class_event_count and is described in Section 7.3.

Table 18 defines the value for pse_assigned_class based on the measured class signatures and class_event_count for single-signature PDs. Table 19 defines the value for pse_assigned_class*X* based on the measured class signatures on each Mode and class_event_count for dual-signature PDs.

Table 18: pse_assigned_class derived from class signatures and class_event_count

PD requested Class	class_sig_A	class_sig_B	class_event_count		pse_assigned_class
Class 1	1	1	1 or more	⇒	1
Class 2	2	2	1 or more	⇒	2
Class 3	3	3	1 or more	⇒	3
Class 4	4	4	1	⇒	3
			2 or more	⇒	4
Class 5	4	0	1	⇒	3
			2 to 3	⇒	4
			4 or more	⇒	5
Class 6	4	1	1	⇒	3
			2 to 3	⇒	4
			4 or more	⇒	6
Class 7	4	2	1	⇒	3
			2 to 3	⇒	4
			4	⇒	6
			5 or more	⇒	7
Class 8	4	3	1	⇒	3
			2 to 3	⇒	4
			4	⇒	6
			5 or more	⇒	8

Table 19: pse_assigned_class$X$ derived from class signatures and class_event_count

PD requested Class (Mode X)	class_sig_A	class_sig_B	class_event_count		pse_assigned_class (Mode X)
Class 1	1	0	1 or more	⇒	1
Class 2	2	0	1 or more	⇒	2
Class 3	3	0	1 or more	⇒	3
Class 4	4	0	1	⇒	3
			2 or more	⇒	4
Class 5	4	3	1	⇒	3
			2 to 3	⇒	4
			4 or more	⇒	5

8 Power via MDI template

The Link Layer Discovery Protocol (LLDP) is a vendor-neutral link layer protocol used by network devices for advertising their identity, capabilities, and neighbors on an IEEE 802 local area network. Using this protocol it is possible for PSEs and PDs to manage all power aspects of PoE. A major element of this is to negotiate power budgets between the PSE and the PD, this is done through DLL (Data Link Layer) Classification. Several other new features are enabled in the new portion of the Power via MDI TLV.

This section describes the basic principles and terminology on which further testing in Section 10 and Section 12 is based.

8.1 Capturing LLDP frames

When a test refers to “capturing LLDP frames”, this includes any received Ethernet frame with Ethertype equal to 0x88CC that has a valid CRC checksum. Any such frames are stored in a list, with the first frame having list index 0, the second frame having list index 1 and so forth. Frames with an invalid CRC checksum are discarded. Additionally, only Ethernet Frames that contain a Power via MDI TLV should be retained. Such frames meet the following:

- Ethertype is 0x88CC
- LLDPDU contains a TLV with type = 127 (refers to a custom TLV)
- The three bytes at offset 0 are 0x00, 0x12, 0x0F (indicates the IEEE 802 identifier)
- The byte at offset 3 is 0x02 (indicates the Power via Medium Dependent Interface) subtype

See Figure 7 for the basic field structure of an Ethernet frame. Preamble and SFD are not shown as these are generally not exposed to the networking stack. Table 20 contains a list of all of the fields and subfields that form the Power via MDI TLV. The “byte offset” in this Table is referenced with zero being the first byte of the Power via MDI TLV The first two bytes (index 0 and 1) are the TLV header for the Power via MDI TLV in the LLDPDU. It is possible that multiple TLV’s are present in the LLDPDU, the index is always that of the Power via MDI TLV. The byte offset is shown in Figure 7.

Fields are byte-aligned in the TLV, whereas subfields are specified by a bit offset. For a given named field, which can consist of any number of bytes, the bit numbering convention is that the most significant bit is on the left. An example of two fields is shown in Figure 8.

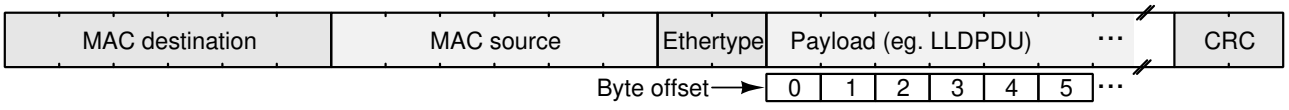

Figure 7: LLDPDU byte offset reference in an Ethernet frame

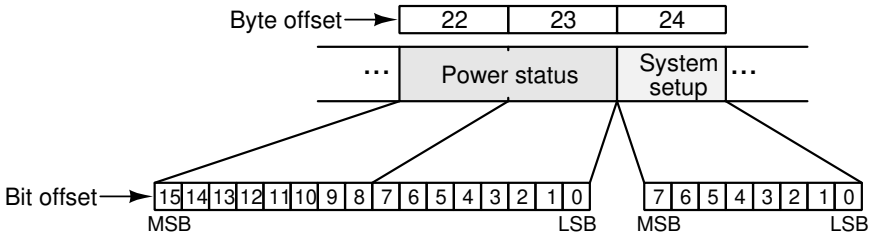

Figure 8: Bit numbering for Power via MDI fields in an LLDPDU

8.2 Default values for outgoing LLDP frames

A Power via MDI LLDP frame has the following default values (which may be overridden in particular tests):

source MAC address is the MAC address of the test device.

destination MAC address is 01:80:c2:00:00:0e.

ethertype is 0x88CC.

frame check sequence field contains a correct CRC code for the given frame.

The payload of the Ethernet frame consists of the following TLVs, in this order:

Chassis ID TLV as described in 8.5.2 of IEEE Std 802.1AB™-2016.

Port ID TLV as described in 8.5.3 of IEEE Std 802.1AB™-2016.

Time to Live TLV as described in 8.5.4 of IEEE Std 802.1AB™-2016, with the TTL value set in the range of 1800 to 3600.

Organizationally specific TLV containing the Power via MDI data, specified further in subsection 8.2.1 and 8.2.2.

End of LLDPDU TLV as described in 8.5.1 of IEEE Std 802.1AB™-2016.

8.2.1 Default values for frames sent to a PSE by the SSPD model

All reserved fields All bits set to zero.

PSE pairs control ability Bit is clear.

PSE MDI power state Bit is clear.

PSE MDI power state Bit is clear.

PSE MDI power support Bit is clear.

Port class Bit is clear.

PSE power pair Field is set to integer value 0.

Power class Field is set to integer value 0.

Power type Bits set to 0b01.

Power source Bits set to 0b00.

PD 4PID Bit is set.

Power priority Bits set to 0b00.

PD requested power value is set according to Table 21. The value is set to 0xACAC when sspd_autoclass is set, or the 'Autoclass request' subfield (see Table 20) is set.

Table 21: PD Requested power value as function of pse_assigned_class

pse_assigned_class	⇒	PD Requested Power value
1		39
2		65
3		130
4		255
5		400
6		510
7		620
8		713

PSE allocated power value When no LLDP Power via MDI frame has been received since power was applied to the SSPD model, the value is the same as the PD requested power value. When LLDP Power via MDI frames have been received, PSE allocated power value is set to the same value as the last received PSE allocated power value in the incoming LLDP Power via MDI frame.

PD requested power value for Mode A is set to zero.

PD requested power value for Mode B is set to zero.

PSE allocated power value for Alternative A is set to zero.

PSE allocated power value for Alternative B is set to zero.

PSE powering status Bits set to 0b00.

PD powered status Bits set to 0b01.

PSE power pairs ext Bits set to 0b00.

Power Class ext This field is set per Table 22.

Table 22: Power class ext as function of pd_req_class

pd_req_class	⇒	Power class ext value
1		0b0001
2		0b0010
3		0b0011
4		0b0100
5		0b0101
6		0b0110
7		0b0111
8		0b1000

Power Type ext If pd_req_class is 6 or less, the bits are 0b010, otherwise the bits are 0b100.

PD Load The bit is clear.

PSE maximum available power value Set to value 0.

Power down request All bits set to 0.

8.2.2 Default values for frames sent to a single-signature PD

All reserved fields All bits set to zero.

PSE pairs control ability Bit is clear.

PSE MDI power state Bit is set.

PSE MDI power support Bit is set.

Port class Bit is set.

PSE power pair If power is applied only on Alternative A or on both Alternatives the value is 1. If power is applied only on Alternative B the value is 2.

Power class Value is as defined in Table 23, depending on the PD requested Class as determined through class_sig_A and class_sig_B in Table 18.

Table 23: Power class as function of PD requested Class

PD requested Class	⇒	Power class value
1		2
2		3
3		4
4		5
5		5
6		5
7		5
8		5

Power type Bits set to 0b00.

Power source Bits set to 0b00.

PD 4PID Bit is clear.

PD requested power value When no LLDP Power via MDI frame has been received since power was applied to the PD, the value is the same as the PSE allocated power value. When LLDP Power via MDI frames have been received, PD requested power value is set to the same value as the last received PD requested power value in the incoming LLDP Power via MDI frame.

PSE allocated power value is set according to Table 24. The value is set to 0xACAC when the 'PSE Autoclass support' field is set and 'Autoclass completed' is set on an outgoing frame (caused by an Autoclass request initiated by the PD).

Table 24: PSE allocated power value as function of pse_assigned_class

pse_assigned_class	⇒	PSE allocated power value
1		39
2		65
3		130
4		255
5		400
6		510
7		620
8		713

PD requested power value for Mode A is set to zero.

PD requested power value for Mode B is set to zero.

PSE allocated power value for Alternative A is set to zero.

PSE allocated power value for Alternative B is set to zero.

PSE powering status When powering in 2-pair mode, the bits are 0b01. When powering in 4-pair mode the bits are 0b10.

PD powered status The bits are 0b00.

PSE power pairs ext If power is applied only on Alternative A (2-pair mode) the bits are set to 0b01. If power is applied only on Alternative B (2-pair mode) the bits are set to 0b10. If power is applied on both Alternatives (4-pair mode) the bits are 0b11.

Power Class ext This field is set per Table 25.

Table 25: Power class ext as function of pse_assigned_class

pse_assigned_class	⇒	Power class ext value
1		0b0001
2		0b0010
3		0b0011
4		0b0100
5		0b0101
6		0b0110
7		0b0111
8		0b1000

Power Type ext If psemodel_max_class is 6 or less, the bits are 0b000, otherwise the bits are 0b001.

PD Load The bit is clear.

PSE maximum available power value The value is set per Table 26.

Table 26: PSE maximum available power value as function of psemodel_max_class

psemodel_max_class	⇒	PSE maximum available power value
1		39
2		65
3		130
4		255
5		400
6		510
7		620
8		713

Power down request The bits are set to 0b000000.

Power down time The integer value is set to 0.

8.3 Template pass requirements for all LLDPDU's

In order to be considered valid, a received LLDPDU must meet all of the following:

1. The destination MAC address is one of 01:80:c2:00:00:00, 01:80:c2:00:00:03, or 01:80:c2:00:00:0e
2. The Power via MDI TLV has a length of 31 bytes (2 bytes for the TLV header, 29 for the TLV information string)
3. The LLDPDU contains a valid TLV type 1 (Chassis ID)
4. The LLDPDU contains a valid TLV type 2 (Port ID)
5. The LLDPDU contains a valid TLV type 3 (Time To Live)
6. The last TLV in the LLDPDU is a type 0 TLV (End of LLDPDU)

8.3.1 Template pass requirements for LLDPDU's sent by a PSE

In addition to passing the requirements of Section 8.3, each of the following items must be as described in order for the LLDPDU to be considered valid:

All reserved fields All bits set to zero.

PSE MDI power state Bit is set.

PSE MDI power support Bit is set.

Port class Bit is set.

PSE power pair If power is applied only on Alternative A the value is 1. If power is applied only on Alternative B the value is 2. If power is applied on both Alternatives the value is 1 or 2.

Power class Value is as defined in Table 27, depending on the assigned class as determined through pse_-assigned_class in Table 18.

Table 27: Power class as function of pse_assigned_class

pse_assigned_class	⇒	Power class value
1		2
2		3
3		4
4 to 8		5

Power type Bits set to 0b00.

Power source Bits set to any combination except 0b11.

PD 4PID Bit is clear.

PD requested power value The integer value is in the range of 0 to 999.

PSE allocated power value The integer value is in the range of 0 to 999.

PD requested power value for Mode A The integer value is in the range of 0 to 499.

PD requested power value for Mode B The integer value is in the range of 0 to 499.

PSE allocated power value for Alternative A The integer value is in the range of 0 to 499.

PSE allocated power value for Alternative B The integer value is in the range of 0 to 499.

PSE powering status When powering in 2-pair mode, the bits are 0b01. When powering in 4-pair mode and the SSPD model is attached, the bits are 0b10. When powering in 4-pair mode and the DSPD model is attached, the bits are 0b11.

PD powered status The bits are 0b00.

PSE power pairs ext If power is applied only on Alternative A the bits are 0b01 and the value of PSE power pair is 1. If power is applied only on Alternative B the bits are 0b10 and the value of PSE power pair is 2. If power is applied on both Alternatives the bits are 0b11.

Power Class ext must match the assigned Class and match the last value of PSE Allocated Power value per Table 28.

Table 28: Power class ext as function of pse_assigned_class and PSE Allocated Power value

pse_assigned_class	PSE Allocated Power Value	⇒	Power class ext value
1	1 to 39		0b0001
2	40 to 65		0b0010
3	66 to 130		0b0011
4	131 to 255		0b0100
5	256 to 400		0b0101
6	401 to 510		0b0110
7	511 to 620		0b0111
8	621 to 999		0b1000

Power Type ext If the PSE Logo Class is 6 or less, the bits are 0b00, otherwise the bits are 0b01.

PD Load The bit is clear.

PSE maximum available power value The integer value is in the range of 1 to 999.

Power down request The bits are 0b000000.

Power down time The integer value is 0.

8.3.2 Template pass requirements for LLDPDU's sent by a single-signature PD

In addition to passing the requirements of Section 8.3, each of the following items must be as described in order for the LLDPDU to be considered valid:

All reserved fields All bits set to zero.

PSE MDI power state Bit is clear.

PSE MDI power support Bit is clear.

Port class Bit is clear.

Power type Bits set to 0b01.

Power source Bits set to any combination except 0b10.

PD 4PID Bit is set.

PD requested power value The integer value is in the range of 0 to 999.

PSE allocated power value The integer value is in the range of 0 to 999.

PD requested power value for Mode A The integer value is in the range of 0 to 499.

PD requested power value for Mode B The integer value is in the range of 0 to 499.

PSE allocated power value for Alternative A The integer value is in the range of 0 to 499.

PSE allocated power value for Alternative B The integer value is in the range of 0 to 499.

PSE powering status The bits are 0b00.

PD powered status For a single-signature PD the bits are 0b01.

PSE power pairs ext The bits are 0b00.

Power Class ext corresponds with the requested Class of the PD as shown in Table 29.

Table 29: Power class as function of PD requested Class

PD requested Class	⇒	Power class value
1		0b0001
2		0b0010
3		0b0011
4		0b0100
5		0b0101
6		0b0110
7		0b0111
8		0b1000

Power Type ext If the PD Logo Class is 6 or less, the bits are 0b010, otherwise the bits are 0b100.

PD Load The bit is clear.

PSE maximum available power value The integer value is in the range of 1 to 999.

Power down request The integer value is 0 or 0x1D.

Table 20: Power via MDI TLV field layout

Field description	Byte offset	# bytes	Bit offset	# bits
TLV header	0	2		
TLV type			15	7
TLV information string length			8	9
Organizationally Unique Identifier	2	3		
IEEE 802.3 subtype	5	1		
MDI power support	6	1		
Reserved			7	4
PSE pairs control ability			3	1
PSE MDI power state			2	1
PSE MDI power support			1	1
Port class			0	1
PSE power pair	7	1		
Power class	8	1		
Type/source/priority	9	1		
Power type			7	2
Power source			5	2
Reserved			3	1
PD 4PID			2	1
Power priority			1	2
PD requested power value	10	2		
PSE allocated power value	12	2		
PD requested power value Mode A	14	2		
PD requested power value Mode B	16	2		
PSE allocated power value Alternative A	18	2		
PSE allocated power value Alternative B	20	2		
Power status	22	2		
PSE powering status			15	2
PD powered status			13	2
PSE power pairs ext			11	2
Dual-signature power Class ext Mode A			9	3
Dual-signature power Class ext Mode B			6	3
Power Class ext			3	4
System setup	24	1		
Reserved			7	4
Power Type ext			3	3
PD Load			0	1
PSE maximum available power	25	2		
Autoclass	27	1		
Reserved			7	5
PSE Autoclass support			2	1
Autoclass completed			1	1
Autoclass request			0	1
Power down	28	3		
Power down request			23	6
Power down time			17	18

9 PSE Test suite

The following tests compose the test plan for PSEs.

9.1 PSE1 PSE polarity configurations

This test is for PICS PSE1, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.4.

> Requirement from IEEE Std 802.3bt™-2018
>
> PSEs shall use only the permitted polarity configurations associated with Alternative A and Alternative B listed in Table 145–4 corresponding with their Type.

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to the PSE Logo Class.

Test procedure:

1. Enable the PSE and wait for it to apply power to the PD.
2. Measure voltage V_{PSEPI_A} and V_{PSEPI_B}.

Pass requirements:

For a Type 3 PSE: Either V_{PSEPI_A} or V_{PSEPI_B} is in the range of 50 V to 57 V [⇨$V_{Port\_PSE\text{-}2P}$, Type 3] in either polarity, or both V_{PSEPI_A} and V_{PSEPI_B} are in the range of 50 V to 57 V [⇨$V_{Port\_PSE\text{-}2P}$, Type 3] in either polarity.

For a Type 4 PSE: Either V_{PSEPI_A} or V_{PSEPI_B} are in the range of 52 V to 57 V [⇨$V_{Port\_PSE\text{-}2P}$, Type 4] in the polarity as indicated in the SSPD test model in Figure 4, or both V_{PSEPI_A} and V_{PSEPI_B} are in the range of 52 V to 57 V [⇨$V_{Port\_PSE\text{-}2P}$, Type 4] in the polarity indicated in the SSPD test fixture.

9.2 PSE2 Alternative implementation

This test is for PICS PSE2, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.4.

Requirement from IEEE Std 802.3bt™-2018
Type 3 PSEs shall implement Alternative A, Alternative B, or both.

Last modification: Initial version.

History of changes: —

Test applicable to: PSE Logo Class of 4 or less

Test setup: Connect the SSPD model to the PSE with pd_req_class set to the PSE Logo Class.

Test procedure:

1. Enable the PSE and wait for it to apply power to the PD.
2. Measure voltage V_{PSEPI_A} and V_{PSEPI_B}.

Pass requirements: Voltage V_{PSEPI_A} or voltage V_{PSEPI_B} is in the range of 50 V to 57 V [⇨$V_{Port\_PSE\text{-}2P}$, Type 3].

9.3 PSE3 Alternative implementation

This test is for PICS PSE3, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.4.

Requirement from IEEE Std 802.3bt™-2018
Type 3 PSEs providing Class 5 or Class 6 power levels and Type 4 PSEs shall implement Alternative A and Alternative B.

Last modification: Initial version.

History of changes: —

Test applicable to: PSE Logo Class 5 or higher.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to the PSE Logo Class.

Test procedure:

1. Enable the PSE and wait for it to apply power to the PD.
2. Measure voltage V_{PSEPI_A} and V_{PSEPI_B}.

Pass requirements: For PSE Logo Class 5 and 6: voltage V_{PSEPI_A} and voltage V_{PSEPI_B} are in the range of 50 V to 57 V [⇨$V_{Port\_PSE\text{-}2P}$, Type 3] , for PSE Logo Class 7 and 8: voltage V_{PSEPI_A} and voltage V_{PSEPI_B} are in the range of 52 V to 57 V [⇨$V_{Port\_PSE\text{-}2P}$, Type 4].

9.4 PSE4 PSE behavior (state diagrams)

This test is for PICS PSE4, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.5.

Requirement from IEEE Std 802.3bt™-2018
PSEs shall provide the behavior of the state diagrams shown in Figure 145–13 to Figure 145–18.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.5 PSE5 PSE performing detection only on Alternative B fails to detect a valid PD detection signature

This test is for PICS PSE5, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.5.1.

Requirement from IEEE Std 802.3bt™-2018

A PSE performing detection using only Alternative B may fail to detect a valid PD detection signature. When this occurs, the PSE shall back off for at least T_{dbo} as defined in Table 145–16 before attempting another detection, except in the case of an open circuit as defined in 145.2.6.5.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.6 PSE6 Backoff voltage

This test is for PICS PSE6, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.5.1.

Requirement from IEEE Std 802.3bt™-2018
During this backoff, the PSE shall not apply a voltage greater than V_{Off} to the PI.

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with the following modification:

- R_{det} is set to any value lower than 0.5 MΩ but not within the range of 15 kΩ to 33 kΩ

Test procedure:

1. Enable the PSE.
2. Measure V_{PSEPI_A} and V_{PSEPI_B} continuously for 5 s.

Pass requirements: V_{PSEPI_B} is less than 2.8 V [⇨V_{Off}] for at least 2000 ms [⇨T_{dbo}] in any window of at least 2500 ms or V_{PSEPI_A} exceeds 2.8 V [⇨V_{Off}] at any time during the measurement.

9.7 PSE7 Alternative roles establishment

This test is for PICS PSE7, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.5.1.

Requirement from IEEE Std 802.3bt™-2018
In any implementation, the roles of the Alternatives shall be established in IDLE and be maintained in every other state.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.8 PSE8 Set pse_avail_pwr, pse_avail_pwr_pri, and pse_avail_pwr_sec

This test is for PICS PSE8, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.5.4.

Requirement from IEEE Std 802.3bt™-2018
PSEs shall set pse_avail_pwr, pse_avail_pwr_pri, and pse_avail_pwr_sec from the range in Table 145–6.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.9 PSE9 Applying operating voltage to a pairset

This test is for PICS PSE9, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.6.

> Requirement from IEEE Std 802.3bt™-2018
>
> The PSE shall not apply operating voltage to a pairset until the PSE has successfully detected a valid signature over that pairset.

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

9.9.1 Test 1 — Bad detection signature A

Test setup: Connect the DSPD model to the PSE with the following modification:

- An invalid detection signature is created on Mode A by at least one of the following:
  - R_{detA} is set higher than 33 kΩ or set lower than 15 kΩ
  - C_{inA} is set higher than 10 µF

Test procedure:

1. Enable the PSE and measure V_{PSEPI_A} continuously for at least 5 s.

Pass requirements: V_{PSEPI_A} does not exceed 30 V [$\Rightarrow V_{oc}$ max].

9.9.2 Test 2 — Bad detection signature B

Test setup: Connect the DSPD model to the PSE with the following modification:

- An invalid detection signature is created on Mode B by at least one of the following:
  - R_{detB} is set higher than 33 kΩ or set lower than 15 kΩ
  - C_{inB} is set higher than 10 µF

Test procedure:

1. Enable the PSE and measure V_{PSEPI_B} continuously for at least 5 s.

Pass requirements: V_{PSEPI_B} does not exceed 30 V [$\Rightarrow V_{oc}$ max].

9.10 PSE10 Detecting PDs

This test is for PICS PSE10, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.6.1.

Requirement from IEEE Std 802.3bt™-2018
The PSE shall detect the PD by probing via the PSE PI.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.11 PSE11 PSE detection signature

This test is for PICS PSE11, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.6.1.

> Requirement from IEEE Std 802.3bt™-2018
>
> The PSE shall present a non-valid PD detection signature as defined in Table 145–22 when probed in either polarity by another PSE.

Last modification: Initial version.

History of changes:

Version 1.1 Better handling of the case where negative detection currents are measured during a test. When any of the measured detection currents is negative, the "if" statement causes the calculated detection resistance to be zero.

Test applicable to: All PSEs.

Test setup: Connect the PSE to a voltage supply connected per Test 1 as defined in Table 30. The PSE is to be powered and enabled.

Test procedure:

1. Set the supply voltage to 2.91 V ± 100 mV.
2. Measure the current sourced by the supply and record as $I_{detect1}$.
3. Measure the supply output voltage and record as $V_{detect1}$.
4. Set the supply voltage to 4.11 V ± 100 mV.
5. Measure the current sourced by the supply and record as $I_{detect2}$.
6. Measure the supply output voltage and record as $V_{detect2}$.
7. Set the supply voltage to 8.8 V ± 100 mV.
8. Measure the current sourced by the supply and record as $I_{detect3}$.
9. Measure the supply output voltage and record as $V_{detect3}$.
10. Set the supply voltage to 10 V ± 100 mV.
11. Measure the current sourced by the supply and record as $I_{detect4}$.
12. Measure the supply output voltage and record as $V_{detect4}$.
13. If $(I_{detect1} < -20\,\mu A)$ or $(I_{detect2} < -20\,\mu A)$:
    $R_{detect1} = 0$
    else:
    $R_{detect1} = |(V_{detect2} - V_{detect1})/(I_{detect2} - I_{detect1})|$
14. If $(I_{detect3} < -20\,\mu A)$ or $(I_{detect4} < -20\,\mu A)$:
    $R_{detect2} = 0$
    else:
    $R_{detect2} = |(V_{detect4} - V_{detect3})/(I_{detect4} - I_{detect3})|$
15. If $(I_{detect1} < -20\,\mu A)$ or $(I_{detect4} < -20\,\mu A)$:
    $R_{detect3} = 0$
    else:
    $R_{detect3} = |(V_{detect4} - V_{detect1})/(I_{detect4} - I_{detect1})|$

16. Set the supply voltage to 0 V.
17. With the supply disconnected, measure the capacitance of the port (connected per Table 30) and record as $C_{detect1}$.
18. ↻ Repeat steps 1 to 16 for each connection configuration listed in Table 30.

Pass requirements:

- Each of the calculated resistances $R_{detect1}$, $R_{detect2}$, and $R_{detect3}$ are less than 12 kΩ or greater than 45 kΩ [⇨R_{detect}] or $C_{detect1}$ is greater than 10 µF.

Table 30: PSE detection signature configurations

Test	Supply positive	Supply negative
1	pair 1	pair 2
2	pair 2	pair 1
3	pair 3	pair 4
4	pair 4	pair 3
5	pair 1 and pair 3	pair 2
6	pair 1 and pair 3	pair 4
7	pair 2 and pair 4	pair 1
8	pair 2 and pair 4	pair 3

9.12 PSE12 Open circuit voltage and short circuit current

This test is for PICS PSE12, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.6.1.

Requirement from IEEE Std 802.3bt™-2018
The open circuit voltage and short circuit current shall meet the specifications in Table 145–7.

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs

9.12.1 Test 1 — Open circuit voltage

Test setup: Connect the SSPD model to the PSE with the following modification:

- Replace R_{det} with an open circuit ($R_{det} > 1\,M\Omega$)

Test procedure:

1. Enable the PSE.
2. Measure V_{PDPI_A} and V_{PDPI_B} continuously for 5 s.

Pass requirements: Absolute value of V_{PDPI_A} and V_{PDPI_B} does not exceed 30 V [$\Rightarrow V_{oc}$ max] at any time during the measurement.

9.12.2 Test 2 — Short circuit current

Test setup: Connect the SSPD model to the PSE with the following modification:

- Replace R_{det} with a short circuit ($R_{det} < 1\,\Omega$)

Test procedure:

1. Enable the PSE.
2. Measure I_{PD} continuously for 5 s.

Pass requirements: The value of I_{PD} does not exceed 5 mA [$\Rightarrow I_{sc}$] at any time during the measurement.

9.13 PSE13 Backdriven current

This test is for PICS PSE13, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.6.1.

Requirement from IEEE Std 802.3bt™-2018
The PSE shall not be damaged by up to 5 mA backdriven current over the range of V_{oc} as defined in Table 145–7.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.14 PSE14 Output capacitance

This test is for PICS PSE14, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.6.1.

Requirement from IEEE Std 802.3bt™-2018
Output capacitance shall be as defined in Table 145–7 when V_{PSE} is in the range of 0 V to V_{valid} max.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.15 PSE15 Detection voltage with a valid PD signature connected

This test is for PICS PSE15, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.6.2.

> Requirement from IEEE Std 802.3bt™-2018
>
> The detection voltage at the PSE PI shall be within the V_{valid} voltage range, as defined in Table 145–7, with a valid PD detection signature connected, as defined in Table 145–21.

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE.

Test procedure:

1. Continuously measure V_{PSEPI}.
2. Enable the PSE and mark this time as t_0.
3. Mark as t_1 the time when V_{PSEPI} exceeds 10 V [⇳V_{valid} max] for the first time after t_0.
4. Mark as t_2 the time when V_{PSEPI} exceeds 15.5 V [⇳V_{Class} min] for the first time after t_1.
5. Mark as t_3 the time when V_{PSEPI} falls below 10 V [⇳V_{valid} max] after t_2.

Pass requirements: All of the following:

- $t_3 - t_2 > 6\,ms$[⇳T_{CEV} min]
- $V_{PSEPI} < 10\,V$[⇳V_{valid} max] between t_0 and $(t_1 - 1\,ms)$

9.16 PSE16 Detection voltage measurements

This test is for PICS PSE16, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.6.2.

Requirement from IEEE Std 802.3bt™-2018

In evaluating the presence of a valid PD, the PSE shall make at least two measurements with V_{PSE} values that create at least a ΔV_{test} difference as defined in Table 145–7.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.17 PSE17 Control slew rate when switching detection voltages

This test is for PICS PSE17, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.6.2.

Requirement from IEEE Std 802.3bt™-2018
The PSE shall control the slew rate of the probing detection voltage when switching between detection voltages to be less than V_{slew} as defined in Table 145–7.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.18 PSE18 Accept as a valid signature

This test is for PICS PSE18, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.6.3.

Requirement from IEEE Std 802.3bt™-2018
A PSE shall accept as a valid PD detection signature a pairset with all of the characteristics specified in Table 145–8.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.19 PSE19 Reject as an invalid signature

This test is for PICS PSE19, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.6.4.

Requirement from IEEE Std 802.3bt™-2018
The PSE shall reject as an invalid detection signature, a pairset which exhibits any of the following characteristics:

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE.

Test procedure:

1. Set R_{det} higher than 33 kΩ [⇨R_{bad} max].
2. Enable the PSE and measure V_{PSEPI} for at least 5 s.
3. Set R_{det} lower than 15 kΩ [⇨R_{bad} min].
4. Measure V_{PSEPI} for at least 5 s.
5. Set R_{det} in the range defined in Table 10 (a valid detection resistance) and set C_{in} to be greater than 10 µF [⇨C_{bad}].
6. Measure V_{PSEPI} for at least 5 s.

Pass requirements: V_{PSEPI} does not exceed 30 V [⇨V_{oc} max] during any of the measurements.

9.20 PSE20 Connection check

This test is for PICS PSE20, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.7.

> Requirement from IEEE Std 802.3bt™-2018
>
> PSEs that will source power on both pairsets shall complete a connection check prior to the classification of a PD as defined in 145.2.8 to determine if the PSE is connected to a single-signature PD configuration, a dual-signature PD configuration, or neither.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.21 PSE21 Open circuit voltage and short circuit voltage during connection check

This test is for PICS PSE21, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.7.

Requirement from IEEE Std 802.3bt™-2018

During connection check the PSE shall meet the specifications for open circuit voltage, V_{oc}, and short circuit current, I_{sc}, in Table 145–7.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.22 PSE22 Connection check voltage when a single- or dual-signature PD is connected

This test is for PICS PSE22, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.7.

Requirement from IEEE Std 802.3bt™-2018
The connection check voltage at the PSE PI shall be within the V_{valid} voltage range, as defined in Table 145–7, when a single-signature PD or a dual-signature PD is connected.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.23 PSE23 Voltage on either pairset rises above V_{valid} max during connection check

This test is for PICS PSE23, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.7.

Requirement from IEEE Std 802.3bt™-2018

If the voltage on either pairset rises above V_{valid} max, as defined in Table 145–7, during connection check, the PSE shall reset the PD by bringing the voltage at the PI below V_{off} max, as defined in Table 145–16, for at least T_{Reset}, as defined in Table 145–14, before performing classification.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.24 PSE24 Channel resistance considerations for $P_{Autoclass}$

This test is for PICS PSE24, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.

Requirement from IEEE Std 802.3bt™-2018

$P_{Autoclass}$ shall be increased by at least P_{ac_margin}, as defined in Table 145–15, in order to account for potential increase in link section resistance due to temperature increase, up to the value defined in Table 145–11 of the Class assigned to the PD, and with a minimum power allocation of Class 1.

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with the following modifications:

- Autoclass is enabled
- Set pd_req_class between 2 and the PSE Logo Class
- Set the power draw of the PD, p_0, such that: $1.5\,W < p_0 < (⇩P_{Class\_PD}$ for pd_req_class $- 1.5\,W)$

Test procedure: Let t_0 be the time when the SSPD turns on. Let p_0 be the initial power level of the PD.

1. Enable the PSE and wait for the PSE to power the PD.
2. At a time greater than $t_0 + 5\,s$, increase the power drawn by the PD to a value between $p_0 + 0.9 \times ⇩P_{ac\_margin}$ and $p_0 + ⇩P_{ac\_margin}$.
3. Wait for at least 2 s.

Assigned Class	1 to 4	5 to 6	7 to 8
$⇩P_{ac\_margin}$ (W)	0.5	0.75	1.5

Pass requirements: PSE continues to power the PD.

9.24a PSE24a Minimum supported output power if $P_{Autoclass}$ is less than or equal to 4 W

This test is for PICS PSE24a, the matching requirement is located in IEEE P802.3cv subclause 145.2.8.

Requirement from IEEE P802.3cv
If $P_{Autoclass}$ is less than or equal to 4 W then the minimum supported output power shall be P_{Class} per the assigned Class.

Last modification: Introduced in version 1.1.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with the following modifications:

- Autoclass is enabled
- Set the power draw of the PD, p_0, such that $1\,W \leq p_0 \leq \Rsh P_{Class\_PD}$ for Class 1
- Set pd_req_class to the PSE Logo Class

Test procedure: Let t_0 be the time when the SSPD turns on. Let p_0 be the initial power level of the PD.

1. Enable the PSE and wait for the PSE to power the PD.
2. At a time greater than $t_0 + 5\,s$, increase the power drawn by the PD to a value between $0.9 \times \Rsh P_{Class\_PD}$ and $\Rsh P_{Class\_PD}$ for pd_req_class.
3. Wait for at least 2 s.

Assigned Class	1	2	3	4	5	6	7	8
$\Rsh P_{Class\_PD}$ (W)	3.84	6.49	13	25.5	40	51	62	71.3

Pass requirements: PSE continues to power the PD.

9.25 PSE25 Power allocation after a fault

This test is for PICS PSE25, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.

Requirement from IEEE Std 802.3bt™-2018

When the PSE assigns Class 5 through 8 prior to a fault and then transitions to PRIMARY_SEMI_PWRON or SECONDARY_SEMI_PWRON, it shall revert the allocation of power to Class 4 and assert local_system_change to update PSEAllocatedPowerValue.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.26 PSE26 Autoclass measurement and 2-pair/4-pair power

This test is for PICS PSE26, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.

Requirement from IEEE Std 802.3bt™-2018

A PSE that measured $P_{Autoclass}$ while providing power over 4 pairs, shall increase the power allocation by at least P_{ac_extra}, as defined in Equation (145–4), when it provides power over 2 pairs.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.27 PSE27 Perform Multiple-Event Physical Layer classification

This test is for PICS PSE27, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.

> Requirement from IEEE Std 802.3bt™-2018
>
> Subsequent to successful detection, PSEs shall perform Multiple-Event Physical Layer classification and may perform Data Link Layer classification.

9.27.1 Test 1 — Single-signature classification

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to 1.

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement.
3. Wait for the PSE to power the PD (or in the specific case that the PSE cannot provide power, until one complete classification sequence is recorded).
4. Record the number of classification events produces by the PSE: class_event_count.
5. ↻ Repeat the test with pd_req_class set to 2, 3, 4, 5, 6, 7, and 8.

Pass requirements: The recorded number of class events produced (class_event_count) conforms to Table 31. PSEs for logo Class 1 or 2 do not apply power when pd_req_class is set higher than the PSE Logo Class.

Table 31: Class event count based on requested Class and PSE Logo Class (single-signature)

	PSE Logo Class							
pd_req_class	1	2	3	4	5	6	7	8
1	1	1	1	1	1	1	1	1
2	—	1	1	1	1	1	1	1
3	—	—	1	1	1	1	1	1
4	—	—	1	2 or 3	2 or 3	2 or 3	2 or 3	2 or 3
5	—	—	1	2 or 3	4	4	4	4
6	—	—	1	2 or 3	2 or 3	4	4	4
7	—	—	1	2 or 3	2 or 3	4	5	5
8	—	—	1	2 or 3	2 or 3	4	4	5

— denotes that power is not applied.

9.27.2 Test 2 — Dual-signature classification

Last modification: Initial version.

History of changes: —

Test applicable to: PSE Logo Class 5 or greater.

Test setup: Connect the DSPD model to the PSE with pd_req_class_modeA and pd_req_class_modeB set to 1.

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement on each pairset.
3. Wait for the PSE to power the PD (or in the specific case that the PSE cannot provide power, until one complete classification sequence is recorded).
4. Record the number of classification events produces by the PSE: class_event_count.
5. ↻ Repeat the test with pd_req_class_modeA and pd_req_class_modeB set to 2, 3, 4, and 5.

Pass requirements: The recorded number of class events produced on each pairset (class_event_count) conforms to Table 32.

Table 32: Class event count based on requested Class and PSE Logo Class (dual-signature)

	PSE Logo Class			
	5	6	7	8
pd_req_class_modeA&B				
1 & 1	1,2, or 3	1,2, or 3	1,2, or 3	1,2, or 3
2 & 2	1,2, or 3	1,2, or 3	1,2, or 3	1,2, or 3
3 & 3	1,2, or 3	1,2, or 3	1,2, or 3	1,2, or 3
4 & 4	1	2 or 3	2 or 3	2 or 3
5 & 5	1	2 or 3	2 or 3	4

9.28 PSE28 Dual-signature classification

This test is for PICS PSE28, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.

Requirement from IEEE Std 802.3bt™-2018
PSEs that will source power over 4-pair to a dual-signature PD shall perform Physical Layer classification on each pairset.

Last modification: Initial version.

History of changes: —

Test setup: Connect the DSPD model to the PSE with pd_req_class_modeA and pd_req_class_modeB set to 1.

Test procedure:

- Enable the PSE.
- Perform a classification waveform measurement on both pairsets.
- Wait at least 10 s after the first pairset is powered for the second pairset to power up.

Pass requirements: If power is applied to both pairsets, then class_event_count for Alternative A and class_event_count for Alternative B need to be at least 1.

9.29 PSE29 Support Multiple-Event Physical Layer Classification

This test is for PICS PSE29, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.

Requirement from IEEE Std 802.3bt™-2018
A PSE shall be capable of assigning the highest Class it can support by means of Multiple-Event Physical Layer classification.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.30 PSE30 Failure to complete classification (single-signature)

This test is for PICS PSE30, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.

Requirement from IEEE Std 802.3bt™-2018
A PSE shall return to IDLE if it fails to complete classification after successfully completing detection of a single-signature PD.

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with the following modification:

- I_{cls1} is set above 51 mA [⇩I_{Class_LIM} min]

Test procedure:

1. Enable the PSE.
2. Measure V_{PSEPI} continuously.
3. Perform a classification waveform measurement (continue the measurement for at least 1 s after $t_{classification\_end}$).
4. Wait at least until the PSE performs at least one classification sequence (class_event_count ≥ 1).

Pass requirements:

- PSE does not apply operating voltage (V_{PSEPI} < 20.5 V [⇩V_{Class} max] at all times)
- V_{PSEPI} is less than 2.8 V [⇩V_{Off}] for at least 15 ms [⇩T_{Reset}] continuously after $t_{classification\_end}$

9.31 PSE31 Failure to complete classification (dual-signature)

This test is for PICS PSE31, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.

> Requirement from IEEE Std 802.3bt™-2018
>
> A PSE shall return to IDLE corresponding to the appropriate Alternative if it successfully completes detection on a pairset of a dual-signature PD but fails to complete classification on that pairset.

Last modification: Initial version.

History of changes: —

Test applicable to: PSE Logo Class 5 or greater.

9.31.1 Test 1 — Class failure on Alt A

Test setup: Connect the DSPD model to the PSE with the following modification:

- I_{cls1A} is set above 51 mA [⇨I_{Class_LIM} min]

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement (continue the measurement for at least 1 s after $t_{classification\_end}$).
3. Wait at least until the PSE performs at least one classification sequence (class_event_count for Mode A ≥ 1).

Pass requirements:

- PSE does not apply operating voltage ($V_{PSEPI\_A} < 20.5$ V [⇨V_{Class} max] at all times)
- V_{PSEPI_A} is less than 2.8 V [⇨V_{Off}] for at least 15 ms [⇨T_{Reset}] continuously after $t_{classification\_end}$

9.31.2 Test 2 — Class failure on Alt B

Test setup: Connect the DSPD model to the PSE with the following modification:

- I_{cls1B} is set above 51 mA [⇨I_{Class_LIM} min]

Test procedure:

1. Enable the PSE
2. Perform a classification waveform measurement (continue the measurement for at least 1 s after $t_{classification\_end}$).
3. Wait at least until the PSE performs at least one classification sequence (class_event_count for Mode B ≥ 1).

Pass requirements:

- PSE does not apply operating voltage ($V_{PSEPI\_B} < 20.5\,V$ [⇨V_{Class} max] at all times)
- V_{PSEPI_B} is less than 2.8 V [⇨V_{Off}] for at least 15 ms [⇨T_{Reset}] continuously after $t_{classification\_end}$

9.32 PSE32 Type 3 PSE class and mark event limit (single-signature)

This test is for PICS PSE32, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.1.

Requirement from IEEE Std 802.3bt™-2018
Type 3 PSEs: shall provide a maximum of four class events and four mark events for single-signature PDs

Last modification: Initial version.

History of changes: —

Test applicable to: Type 3 PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to 8.

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement.

Pass requirements: class_event_count is 4 or less.

9.33 PSE33 Type 3 PSE class and mark event limit (dual-signature)

This test is for PICS PSE33, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.1.

Requirement from IEEE Std 802.3bt™-2018
Type 3 PSEs: shall provide a maximum of three class events and three mark events on each pairset for dual-signature PDs

Last modification: Initial version.

History of changes: —

Test applicable to: Type 3 PSEs.

Test setup: Connect the DSPD model to the PSE with pd_req_class_modeA and pd_req_class_modeB set to 5.

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement on each pairset.

Pass requirements: class_event_count is 3 or less.

9.34 PSE34 Type 4 PSE class and mark event limit (single-signature)

This test is for PICS PSE34, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.1.

Requirement from IEEE Std 802.3bt™-2018
Type 4 PSEs: shall provide a maximum of five class events and five mark events for single-signature PDs

Last modification: Initial version.

History of changes: —

Test applicable to: Type 4 PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to the PSE Logo Class (must be 7 or 8 for a Type 4 PSE).

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement.

Pass requirements: class_event_count is 5 or less.

9.35 PSE35 Type 4 PSE class and mark event limit (dual-signature)

This test is for PICS PSE35, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.1.

Requirement from IEEE Std 802.3bt™-2018
Type 4 PSEs: shall provide a maximum of four class events and four mark events on each pairset for dual-signature PDs

Last modification: Initial version.

History of changes: —

Test applicable to: Type 4 PSEs.

Test setup: Connect the DSPD model to the PSE with pd_req_class_modeA and pd_req_class_modeB set to 5.

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement on each pairset.

Pass requirements: class_event_count is 4 or less.

9.36 PSE36 Number of class events based on assigned Class (single-signature)

This test is for PICS PSE36, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.1.

Requirement from IEEE Std 802.3bt™-2018

PSEs connected to a single-signature PD shall issue no more class events than the Class they are able to support and no more than:

- one class event when the PD requests Class 0 through 3
- three class events when the PD requests Class 4
- four class events when the PD requests Class 5 or 6
- five class events when the PD requests Class 7 or 8

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.37 PSE37 Number of class events based on assigned Class (dual-signature)

This test is for PICS PSE37, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.1.

Requirement from IEEE Std 802.3bt™-2018
PSEs connected to a dual-signature PD shall issue, for a given pairset, no more class events than the Class they are able to support and no more than: – three class events when the PD requests Class 1 through 4 on the given pairset – four class events when the PD requests Class 5 on the given pairset

Last modification: Initial version.

History of changes: —

9.37.1 Test 1 — Class 1 to 4

Test setup: Connect the DSPD model to the PSE with pd_req_class_modeA and pd_req_class_modeB set to 4.

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement on both pairsets.

Pass requirements: class_event_count is equal or less than 3 for both pairsets.

9.37.2 Test 2 — Class 5

Test setup: Connect the DSPD model to the PSE with pd_req_class_modeA and pd_req_class_modeB set to 5.

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement on both pairsets.

Pass requirements: class_event_count is equal or less than 4 for both pairsets.

9.38 PSE38 Long class event voltage / timing

This test is for PICS PSE38, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.1.

Requirement from IEEE Std 802.3bt™-2018
When the PSE is in CLASS_EV1_LCE, CLASS_EV1_AUTO, CLASS_EV1_LCE_PRI, CLASS_EV1_-LCE_SEC, CLASS_EV1_LCE_4PID_PRI, or CLASS_EV1_LCE_4PID_SEC, it shall provide to the PI or pairset V_{Class}, subject to T_{LCE} timing specification.

Last modification: Initial version.

History of changes: —

9.38.1 Test 1 — Single-signature PDs

Test setup: Connect the SSPD model to the PSE with pd_req_class set to 1.

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement.

Pass requirements: T_{Class1} is in the range of 88 ms to 105 ms [⇨T_{LCE}].

9.38.2 Test 2 — Dual-signature PDs

Test setup: Connect the DSPD model to the PSE with pd_req_class_modeA and pd_req_class_modeB set to 1.

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement on each pairset.

Pass requirements: For each pairset that perform a classification sequence, T_{Class1} is in the range of 88 ms to 105 ms [⇨T_{LCE}].

9.39 PSE39 Measure I_{Class} in CLASS_EV1_AUTO

This test is for PICS PSE39, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.1.

Requirement from IEEE Std 802.3bt™-2018
The PSE in CLASS_EV1_AUTO shall measure I_{Class} on the negative pair or pairs after T_{Class_ACS}, referenced from the application of the first class event, to determine if the PD will perform Autoclass.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.40 PSE40 Class event voltage / timing

This test is for PICS PSE40, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.1.

> Requirement from IEEE Std 802.3bt™-2018
>
> When the PSE is in CLASS_EV2, CLASS_EV2_PRI, CLASS_EV2_SEC, CLASS_EV3, CLASS_EV3_-PRI, CLASS_EV3_SEC, CLASS_EV4, CLASS_EV4_PRI, CLASS_EV4_SEC, or CLASS_EV5, it shall provide to the PI or pairset V_{Class}, subject to the T_{CEV} timing specification.

Last modification: Initial version.

History of changes: —

9.40.1 Test 1 — Single-signature PDs

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to the PSE Logo Class.

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement.

Pass requirements: For any class events generated (if the class event does not exist, the requirement is not applicable):

- T_{Class2} is in the range of 6 ms to 20 ms [⇨T_{CEV}]
- T_{Class3} is in the range of 6 ms to 20 ms [⇨T_{CEV}]
- T_{Class4} is in the range of 6 ms to 20 ms [⇨T_{CEV}]
- T_{Class5} is in the range of 6 ms to 20 ms [⇨T_{CEV}]

9.40.2 Test 2 — Dual-signature PDs

Test applicable to: PSE Logo Class 5 and greater.

Test setup: Connect the DSPD model to the PSE with pd_req_class_modeA and pd_req_class_modeB set to the corresponding value per the PSE Logo Class (see Table 2).

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement on each pairset.

Pass requirements: For any class events generated on either pairset (if the class event does not exist, the requirement is not applicable):

- T_{Class2} is in the range of 6 ms to 20 ms [⇨T_{CEV}]
- T_{Class3} is in the range of 6 ms to 20 ms [⇨T_{CEV}]
- T_{Class4} is in the range of 6 ms to 20 ms [⇨T_{CEV}]

9.41 PSE41 I_{Class} measurement

This test is for PICS PSE41, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.1.

Requirement from IEEE Std 802.3bt™-2018
In all CLASS states except CLASS_EV1_AUTO, the PSE shall measure I_{Class} on the negative pair or pairs after T_{Class}.

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to the PSE Logo Class with the following modification:

- Whenever present_class_sig_A or present_class_sig_B (see Table 11) is set to TRUE, this will cause one of the classification current sources I_{cls1} through I_{cls6} to become enabled
- Let the moment where present_class_sig_A or present_class_sig_B is set to TRUE be t_0. Between t_0 and $t_0 + 5$ ms the current setting for I_{cls1}, I_{cls2}, I_{cls3}, I_{cls4}, I_{cls5}, and I_{cls6} is set to less than 1 mA.
- At the latest at $t_0 + 6$ ms the current is set to the value required by Table 10

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement.

Pass requirements: The PSE provides the following number of class events:

- For PSE Logo Class 3 or less: 1 event
- For PSE Logo Class 4: 2 or 3 events
- For PSE Logo Class 5 or Class 6: 4 events
- For PSE Logo Class 7 or Class 8: 5 events

9.42 PSE42 Mark event voltage

This test is for PICS PSE42, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.1.

> Requirement from IEEE Std 802.3bt™-2018
>
> When the PSE is in MARK_EV1, MARK_EV1_PRI, MARK_EV1_SEC, MARK_EV2, MARK_EV2_-PRI, MARK_EV2_SEC, MARK_EV3, MARK_EV3_PRI, MARK_EV3_SEC, or MARK_EV4, it shall provide to the PI or pairset V_{Mark}.

Last modification: Initial version.

History of changes: —

9.42.1 Test 1 — Single-signature PDs

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to the PSE Logo Class.

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement.

Pass requirements: V_{PSEPI} is in the range of 7 V to 10 V [⇳V_{Mark}] during T_{Mark1}, T_{Mark2}, T_{Mark3}, T_{Mark4}, and T_{Mark5}. For T_{Mark2} through T_{Mark5} this can only be verified if the PSE produces those mark events. This does not apply to the last mark event (the one ending at $t_{classification\_end}$).

9.42.2 Test 2 — Dual-signature PDs

Test applicable to: PSE Logo Class 5 and greater.

Test setup: Connect the DSPD model to the PSE with pd_req_class_modeA and pd_req_class_modeB set to the corresponding value per the PSE Logo Class (see Table 2).

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement on each pairset.

Pass requirements: V_{PSEPI_A} and V_{PSEPI_B} are in the range of 7 V to 10 V [⇳V_{Mark}] during T_{Mark1}, T_{Mark2}, T_{Mark3}, and T_{Mark4}. For T_{Mark2} through T_{Mark4} this can only be verified if the PSE produces this many mark events. This does not apply to the last mark event (the one ending at $t_{classification\_end}$).

9.43 PSE43 Mark event timing

This test is for PICS PSE43, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.1.

Requirement from IEEE Std 802.3bt™-2018
The timing specification shall be as defined by T_{ME1}.

Last modification: Initial version.

History of changes: —

9.43.1 Test 1 — Single-signature PDs

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with the requested Class set to the PSE Logo Class.

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement.

Pass requirements: For any mark event that is generated by the PSE, and is not the last mark (the one ending at $t_{classification\_end}$): T_{Mark1}, T_{Mark2}, T_{Mark3}, and T_{Mark4}, are all in the range of 6 ms to 12 ms [⇳T_{ME1}].

9.43.2 Test 2 — Dual-signature PDs

Test applicable to: PSE Logo Class 5 and greater.

Test setup: Connect the DSPD model to the PSE with pd_req_class_modeA and pd_req_class_modeB set to the corresponding value per the PSE Logo Class (see Table 2).

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement on each pairset.

Pass requirements: For any mark event that is generated by the PSE on either pairset, and is not the last mark (the one ending at $t_{classification\_end}$): T_{Mark1}, T_{Mark2}, and T_{Mark3}, are all in the range of 6 ms to 12 ms [⇳T_{ME1}].

9.44 PSE44 Last mark event voltage

This test is for PICS PSE44, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.1.

Requirement from IEEE Std 802.3bt™-2018
When a PSE is in MARK_EV_LAST, MARK_EV_LAST_PRI or MARK_EV_LAST_SEC, it shall provide to the PI or pairset V_{Mark}.

Last modification: Initial version.

History of changes: —

9.44.1 Test 1 — Single-signature PDs

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with the requested Class set to the PSE Logo Class.

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement.

Pass requirements: V_{PSEPI} is in the range of 7 V to 10 V [⇩V_{Mark}] during the last mark event, the one immediately preceding $t_{classification\_end}$.

9.44.2 Test 2 — Dual-signature PDs

Test applicable to: PSE Logo Class 5 and greater.

Test setup: Connect the DSPD model to the PSE with pd_req_class_modeA and pd_req_class_modeB set to the corresponding value per the PSE Logo Class (see Table 2).

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement on each pairset.

Pass requirements: V_{PSEPI_A} and V_{PSEPI_B} are in the range of 7 V to 10 V [⇩V_{Mark}] during the last mark event on each pairset, the one immediately preceding $t_{classification\_end}$. This only applies when the PSE performs a classification sequence on a pairset. At least one pairset must perform a classification sequence.

9.45 PSE45 Last mark event timing

This test is for PICS PSE45, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.1.

Requirement from IEEE Std 802.3bt™-2018
The timing specification shall be as defined by T_{ME2}.

Last modification: Initial version.

History of changes: —

9.45.1 Test 1 — Single-signature PDs

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with the requested Class set to the PSE Logo Class.

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement.

Pass requirements: The last mark event, the one ending at $t_{classification\_end}$, has a duration of at least 6 ms [⇳T_{ME2}].

9.45.2 Test 2 — Dual-signature PDs

Test applicable to: PSE Logo Class 5 and greater.

Test setup: Connect the DSPD model to the PSE with pd_req_class_modeA and pd_req_class_modeB set to the corresponding value per the PSE Logo Class (see Table 2).

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement on each pairset.

Pass requirements: The last mark event on each pairset that performs a classification sequence, the one ending at $t_{classification\_end}$, has a duration of at least 6 ms [⇳T_{ME2}].

9.46 PSE46 I_{Class} exceeds I_{Class_LIM} min

This test is for PICS PSE46, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.1.

Requirement from IEEE Std 802.3bt™-2018
If any measured I_{Class} is equal to or greater than I_{Class_LIM} min, a PSE shall return to IDLE.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.47 PSE47 Class event currents

This test is for PICS PSE47, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.1.

Requirement from IEEE Std 802.3bt™-2018
The PSE shall limit class event currents to I_{Class_LIM} ...

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with the following modification:

- I_{cls1} is set above 110 mA

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement and measure the maximum current.

Pass requirements: The measured maximum current is less than 100 mA [⇨I_{Class_LIM} max].

9.48 PSE48 Mark event currents

This test is for PICS PSE48, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.1.

Requirement from IEEE Std 802.3bt™-2018
. . . and shall limit mark event currents to I_{Mark_LIM}.

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with the following modification:

- I_{mrk} is set above 110 mA

Test procedure:

1. Enable the PSE.
2. During the classification waveform measurement, measure I_{PD} no more than 5 ms after the start of T_{Mark1}.
3. Perform a classification waveform measurement.

Pass requirements: The current during the mark event is limited below 100 mA [⇨I_{Class_LIM} max].

9.49 PSE49 Class event and mark event voltages polarity

This test is for PICS PSE49, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.1.

Requirement from IEEE Std 802.3bt™-2018
All class event voltages and mark event voltages shall have the same polarity as defined for $V_{Port\_PSE\text{-}2P}$ in 145.2.4.

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connect the DSPD model to the PSE.

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement.
3. Wait for the PSE to provide power on at least one pairset.
4. Measure V_{PSEPI_A} and V_{PSEPI_B}.

Pass requirements: The polarity of each class and mark event on a given pairset is the same as the polarity of the corresponding V_{PSEPI_A} and V_{PSEPI_B}.

9.50 PSE50 Transition from classification to power on

This test is for PICS PSE50, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.1.

> Requirement from IEEE Std 802.3bt™-2018
>
> The PSE shall complete Multiple-Event Physical Layer classification and transition to POWER_ON, POWER_ON_PRI, or POWER_ON_SEC without allowing the voltage at the PI or pairset to go below V_{Mark} min, unless in CLASS_RESET, CLASS_RESET_PRI, or CLASS_RESET_SEC.

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connected the SSPD model to the PSE.

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement.

Pass requirements: Both of the following:

- V_{PSEPI} is greater than 7 V [⇳V_{Mark} min] at all times between $t_{classification\_start}$ and $t_{classification\_end}$
- class_event_count ≥ 1

This requirement only holds when the PSE proceeds to POWER_UP per Figure 6.

9.51 PSE51 PSE returns to IDLE

This test is for PICS PSE51, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.1.

> Requirement from IEEE Std 802.3bt™-2018
>
> If the PSE returns to IDLE, it shall maintain the PI voltage in the range of V_{Reset} for a period of at least T_{Reset} min before starting a new detection cycle.

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with R_{det} set lower than 15 kΩ [⇩R_{bad} min] or higher than 33 kΩ [⇩R_{bad} max].

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measure (continuously).
3. Wait for at least 2 s.
4. Set R_{det} to a valid detection signature value (see Table 9) and mark the time as t_0.

Pass requirements: Between (t_0 − 15 ms) and $t_{classification\_start}$ there is a period of at least 15 ms [⇩T_{Reset}] where V_{PSEPI} is less than 2.8 V [⇩V_{Reset} max].

9.52 PSE52 PI or pairset voltage during class reset

This test is for PICS PSE52, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.1.

Requirement from IEEE Std 802.3bt™-2018
If the PSE is in any of the CLASS_RESET states it shall maintain the PI or pairset voltage in the range of V_{Reset} for a period of at least T_{Reset} min.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.53 PSE53 Dual-signature 4PID with Class 3 or less power available

This test is for PICS PSE53, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.1.

Requirement from IEEE Std 802.3bt™-2018

A PSE that implements 4PID based on Physical Layer classification and is restricted to Class 3 power or less, when connected to a dual-signature PD, shall issue three initial class events to determine the Type of the connected PD, then transition to either CLASS_RESET_PRI or CLASS_RESET_SEC.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.54 PSE54 pd_autoclass is TRUE when PSE reaches POWER_ON

This test is for PICS PSE54, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.2.

Requirement from IEEE Std 802.3bt™-2018
If the PSE implements Autoclass it shall measure $P_{Autoclass}$ when it reaches POWER_ON and pd_autoclass is TRUE.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.55 PSE55 $P_{Autoclass}$ power consumption

This test is for PICS PSE55, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.8.2.

> Requirement from IEEE Std 802.3bt™-2018
>
> The power consumption shall be defined as the highest average power measured throughout the period bounded by T_{AUTO_PSE1} and T_{AUTO_PSE2}.

Last modification: Initial version.

History of changes: —

Test applicable to: PSE Logo Class 3 or greater.

Test setup: Connect the SSPD model to the PSE, with the following modifications:

- Autoclass is enabled

Test procedure: Let t_0 be the time where the SSPD turns on, let p_0 and p_1 be two power levels, with a difference of at least 5 W, both less than ΦP_{Class_PD} for the assigned Class, but greater than 4 W, and p_1 being the greater power level.

1. Enable the PSE.
2. At $t_0 + 500$ ms set the input power of the SSPD to be p_0.
3. At any time between $t_0 + 1700$ ms and $t_0 + 2700$ ms, change the power draw to p_1 for a time duration of 300 ms to 400 ms, then revert back to power level p_0.
4. At $t_0 + 5000$ ms change the input power to power level p_1.

Pass requirements: PSE continues to provide power.

9.56 PSE56 Applying 4-pair power

This test is for PICS PSE56, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.9.

> Requirement from IEEE Std 802.3bt™-2018
>
> A PSE shall not apply 4-pair power unless the PSE has detected a valid detection signature on both pairsets and one or more of the following conditions are met:
> – The connected PD is a single-signature PD
> – The PSE detects a valid detection signature on the unpowered pairset when power is provided in 2-pair mode
> – The PSE has identified the PD as Type 3 or Type 4

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

9.56.1 Test 1 — bad detection signature A

Test setup: Connect the DSPD model to the PSE with the following modification:

- An invalid detection signature is created on Mode A by at least one of the following:
  - R_{detA} is set higher than 33 kΩ [⇳R_{bad} max] or set lower than 15 kΩ [⇳R_{bad} min]
  - C_{inA} is set higher than 10 µF [⇳C_{bad}]

Test procedure:

1. Measure V_{PSEPI_A} continuously.
2. Enable the PSE and wait for it to apply power to the PD test fixture on either Mode, or at least 10 s (whichever is first).

Pass requirements: V_{PSEPI_A} is less than 30 V [⇳V_{oc} max].

9.56.2 Test 2 — bad detection signature B

Test setup: Connect the DSPD model to the PSE with the following modification:

- An invalid detection signature is created on Mode B by at least one of the following:
  - R_{detB} is set higher than 33 kΩ [⇳R_{bad} max] or set lower than 15 kΩ [⇳R_{bad} min]
  - C_{inB} is set higher than 10 µF [⇳C_{bad}]

Test procedure:

1. Measure V_{PSEPI_B} continuously.
2. Enable the PSE and wait for it to apply power to the PD test fixture on either Mode, or at least 10 s (whichever is first).

Pass requirements: V_{PSEPI_B} is less than 30 V [⇳V_{oc} max].

9.56.3 Test 3 — detection signature on non-powered pairset

Test setup: Connect the DSPD model to the PSE with the following modification:

- pd_req_class_modeA and pd_req_class_modeB are set to 4
- I_{cls3A}, I_{cls3B}, I_{cls4A}, I_{cls4B}, I_{cls5A}, and I_{cls5B} are set in the range of 26 mA to 30 mA
- Behavior change: when S_{2A} closes, S_{1B} opens
- Behavior change: when S_{2B} closes, S_{1A} opens

Test procedure:

1. Measure V_{PSEPI_A} and V_{PSEPI_B} continuously.
2. Enable the PSE and wait for it to apply power to the PD test fixture.

Pass requirements: V_{PSEPI_A}, V_{PSEPI_B}, or both are less than 30 V [$\eth V_{oc}$ max].

9.57 PSE57 Power supply output

This test is for PICS PSE57, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.

Requirement from IEEE Std 802.3bt™-2018
When the PSE provides power to the PI, it shall conform with Table 145–16.

Last modification: Initial version.

History of changes: —

9.57.1 Test 1 — $V_{Port\_PSE\text{-}2P}$

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to 1 and with (R_{pair1}, R_{pair2}, R_{pair3}, and R_{pair4}) in the range of 5 Ω to 6.25 Ω. Note that the requirements in Section 5.1 regarding the connection between the DUT and the test fixture apply.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Adjust P_{load} such that $V_{SSPD} \times I_{PD} = ⇳P_{Class\_PD}$ for the assigned Class.
3. Confirm the PSE maintains power.
4. ↻ Repeat the test with pd_req_class set to 2, 3, 4, 5, 6, 7, and 8.

Pass requirements:

- For a Type 3 PSE: V_{PSEPI} is in the range of 50 V to 57 V [$⇳V_{Port\_PSE\text{-}2P}$, Type 3]
- For a Type 4 PSE: V_{PSEPI} is in the range of 52 V to 57 V [$⇳V_{Port\_PSE\text{-}2P}$, Type 4]

9.57.2 Test 2 — $V_{Port\_PSE\_diff}$

Test applicable to: PSE Logo Class 5 or greater

Test setup: Connect the SSPD model to the PSE with pd_req_class set to Class 5.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Confirm the PSE has assigned Class 5 (class_event_count = 4).
3. Set P_{load} such that I_{PD} is 0 mA and mark the time as t_0.
4. Measure the voltage between the positive pair of Alternative A (Pair 1 or Pair 2 on the PSE PI) and the positive pair of Alternative B (Pair 3 or Pair 4).
5. Measure the voltage between the negative pair of Alternative A (Pair 1 or Pair 2 on the PSE PI) and the negative pair of Alternative B (Pair 3 or Pair 4).

NOTE — The measurement must be completed within 300 ms of P_{load} being set to 0 mA.

Pass requirements: The two measured voltages are less than 10 mV [⇩$V_{Port\_PSE\_diff}$].

9.57.3 Test 3 — $V_{Tran\text{-}2P}$

Test applicable to: No test is required.

9.57.4 Test 4 — V_{noise}

Test applicable to: No test is required.

9.57.5 Test 5 — $I_{Con\text{-}2P\text{-}unb}$

Test applicable to: No test is required.

9.57.6 Test 6 — I_{Inrush}

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to Class 4 or less and the following modifications:

- Value of C_{bulk} is limited to 5 µF
- The behavior is modified to bypass the SSPD inrush limiter as defined in Table 33
- A voltage limiting element is placed in parallel with C_{bulk}, with a voltage limit between 30 V to 36 V

Table 33: SSPD behavior modification for PSE57 — Test 6

State diagram variable			SSPD model element
pd_max_power			
	inrush	⇒	S_2 = closed, $I_{inrushlim}$ = 0 mA

Test procedure:

1. Measure V_{PSEPI} continuously and mark as t_0 the time when V_{PSEPI} crosses 30 V after S_2 is closed.
2. Measure I_{PD} continuously.
3. Enable the PSE and measure for 100 ms after t_0.
4. ↻ Repeat the test with pd_req_class set to 5, 7, and the PSE Logo Class.

Pass requirements: I_{PD} is in the range of [⇩I_{Inrush}] for the assigned Class between t_0 and $t_0 + 50$ ms.

Assigned Class	1 to 4	5 to 6	7 to 8
⇩I_{Inrush} (mA)	400 – 450	400 – 900	800 – 900

9.57.7 Test 7 — $I_{Inrush\text{-}2P}$ single-signature

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to Class 4 or less and the following modifications:

- Value of C_{bulk} is limited to 5 µF
- The behavior is modified to bypass the SSPD inrush limiter as defined in Table 33
- A voltage limiting element is placed in parallel with C_{bulk}, with a voltage limit between 30 V to 36 V

Test procedure:

1. Measure V_{PSEPI} continuously and mark as t_0 the time when V_{PSEPI} crosses 30 V after S_2 is closed.
2. Measure I_{PDA} and I_{PDB}
3. Enable the PSE and measure for 100 ms after t_0.
4. ↻ Repeat the test with pd_req_class set to 5 and 7.

Pass requirements: I_{PDA} and I_{PDB} are less than [⇩$I_{Inrush\text{-}2P}$] for the assigned Class between t_0 and $t_0 + 50$ ms.

Assigned Class	1 to 4	5 to 8
⇩$I_{Inrush\text{-}2P}$ (single-signature) (mA)	450	600

9.57.8 Test 8 — $I_{Inrush\text{-}2P}$ dual-signature

Test applicable to: PSE Logo Class 5 or greater

Test setup: Connect the DSPD model to the PSE with the following modifications:

- Value of C_{bulkA} and C_{bulkB} is limited to 5 µF
- The behavior is modified to bypass the DSPD inrush limiter as defined in Table 34
- Voltage limiting elements are placed in parallel with C_{bulkA} and C_{bulkB}, with a voltage limit between 30 V to 36 V

Table 34: DSPD behavior modification for PSE57 — Test 8

State diagram variable			DSPD model element
pd_max_power_modeA	inrush	⇒	S_{2A} = closed, $I_{inrushlimA}$ = 0 mA
pd_max_power_modeB	inrush	⇒	S_{2B} = closed, $I_{inrushlimB}$ = 0 mA

Test procedure:

1. Measure V_{PSEPI_A} continuously and mark as t_0 the time when V_{PSEPI_A} crosses 30 V after S_{2A} is closed.
2. Measure V_{PSEPI_B} continuously and mark as t_1 the time when V_{PSEPI_B} crosses 30 V after S_{2B} is closed.
3. Measure I_{PDA} and I_{PDB} continuously.
4. Enable the PSE and measure for 100 ms after the greater of t_0 and t_1.

Pass requirements:

- I_{PDA} is in the range of 400 mA to 450 mA [⇳$I_{Inrush\text{-}2P}$] from t_0 to $t_0 + 50$ ms
- I_{PDB} is in the range of 400 mA to 450 mA [⇳$I_{Inrush\text{-}2P}$] from t_1 to $t_1 + 50$ ms

9.57.9 Test 9 — T_{Inrush}

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE.

Test procedure:

1. Measure I_{PD} continuously.
2. Mark as t_0 the time when V_{PSEPI} crosses 30 V after S_2 is closed.
3. Set P_{load} such that it attempts to draw I_{PD} = ⇳I_{Inrush} max + 100 mA.
4. Enable the PD and measure for at least 100 ms after t_0.

Pass requirements: The PSE turns off power within $t_0 + 50$ ms to $t_0 + 75$ ms [⇳T_{Inrush}].

9.57.10 Test 10 — $I_{CUT\text{-}2P}$

Test applicable to: No test is required.

9.57.11 Test 11 — T_{CUT}

Test applicable to: No test is required.

9.57.12 Test 12 — $I_{LIM\text{-}2P}$

Test applicable to: No test is required.

9.57.13 Test 13 — T_{LIM}

Test applicable to: No test is required.

9.57.14 Test 14 — P_{Type}

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set the to PSE Logo Class and with (R_{pair1}, R_{pair2}, R_{pair3}, and R_{pair4}) in the range of 5 Ω to 6.25 Ω. Note that the requirements in Section 5.1 regarding the connection between the DUT and the test fixture apply.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Adjust P_{load} such that $V_{SSPD} \times I_{PD} = \Rightarrow P_{Class\_PD}$ for pd_req_class.
3. Wait for at least 5 s.

Assigned Class	1	2	3	4	5	6	7	8
$\Rightarrow P_{Class\_PD}$ (W)	3.84	6.49	13	25.5	40	51	62	71.3

Pass requirements: PSE maintains power.

9.57.15 Test 15 — T_{pon}

Test applicable to: No test is required.

9.57.16 Test 16 — T_{Rise}

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE.

Test procedure:

1. Measure V_{PSEPI} continuously.
2. Perform a classification waveform measurement.
3. Mark as t_0 the moment when V_{PSEPI} exceeds 10 V [$\Rightarrow V_{Mark}$ max] for the last time before $t_{classification\_end}$.
4. Measure V_{PSEPI} at $t_0 + 100$ ms, record this as V_{final}.
5. Mark as t_1 the moment when V_{PSEPI} equals 90% of V_{final} after t_0.
6. Enable the PSE and wait until the PD test fixture is powered up, while performing the measurements described in the previous steps.

Pass requirements: $t_1 - t_0 \geq 15\,\mu s$[$\Rightarrow T_{Rise}$].

9.57.17 Test 17 — T_{Off}

Test applicable to: No test is required.

9.57.18 Test 18 — V_{Off}

Test applicable to: No test is required.

9.57.19 Test 19 — $I_{Hold\text{-}2P}$

Test applicable to: No test is required.

9.57.20 Test 20 — I_{Hold}

Test applicable to: No test is required.

9.57.21 Test 21 — T_{MPDO}

Test applicable to: No test is required.

9.57.22 Test 22 — T_{MPS}

Test applicable to: No test is required.

9.57.23 Test 23 — T_{dbo}

Test applicable to: No test is required.

9.57.24 Test 24 — T_{det}

Test applicable to: No test is required.

9.57.25 Test 25 — T_{ed}

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Measure V_{PSEPI} continuously.
3. Set P_{load} to a value greater than 105 W.
4. Mark as t_0 the time when V_{PSEPI} is less than 0 V to 2.8 V [⇨V_{Reset}].
5. Mark as t_1 the time when V_{PSEPI} exceeds 30 V. The measurement may be stopped 2 s after t_0.

Pass requirements: The difference between t_1 and t_0 is greater than 750 ms [⇨T_{ed}], or the PSE does not re-apply power during the measurement.

9.58 PSE58 Output voltage regulation

This test is for PICS PSE58, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.1.

> Requirement from IEEE Std 802.3bt™-2018
>
> The specification for $V_{Port\_PSE\text{-}2P}$ in Table 145–16 shall be met with a load step of (I_{Hold} max * $V_{Port\_PSE\text{-}2P}$ min) to the maximum power per the PSE's assigned Class at a rate of change of up to 15 mA/µs.

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to the PSE Logo Class.

Test procedure:

1. Enable to the PSE and wait for the PD test fixture to be powered up.
2. Set P_{load} between 2 W to 4 W.
3. Measure V_{PSEPI} continuously.
4. Ramp up P_{load} to any power value between $0.9 \times \Rightarrow P_{Class\_PD}$ and $\Rightarrow P_{Class\_PD}$, with the ramp up completed in no less than 120 µs and no more than 1 ms.

Pass requirements: The measured V_{PSEPI} is within the $\Rightarrow V_{Port\_PSE\text{-}2P}$ range at all times for the given PSE Type.

PSE Type	Type 3	Type 4
$\Rightarrow V_{Port\_PSE\text{-}2P}$ (V)	50 – 57	52 – 57

9.59 PSE59 Voltage transients

This test is for PICS PSE59, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.1.

Requirement from IEEE Std 802.3bt™-2018
The voltage transients as a result of load changes up to 35 mA/µs shall be limited to 3.5 V/µs.

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to the PSE Logo Class.

Test procedure:

1. Enable to the PSE and wait for the PD text fixture to be powered up.
2. Measure V_{PSEPI} continuously.
3. Ramp ⇳P_{load} up or down such that the rate of change in current of I_{PD} is in the range of 20 mA/µs and 35 mA/µs.

Pass requirements: The rate of voltage change of V_{PSEPI} is below 3.5 V/µs.

9.60 PSE60 4-pair power for assigned Class 5 to 8

This test is for PICS PSE60, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.1.

Requirement from IEEE Std 802.3bt™-2018
A PSE that has assigned Class 5 to 8 to a single-signature PD shall apply power to both pairsets while in POWER_ON.

Last modification: Initial version.

History of changes: —

Test applicable to: PSE Logo Class 5 or greater.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to 5.

Test procedure:

1. Enable to the PSE.
2. Perform a classification waveform measurement.
3. Wait for the PD to be powered up.
4. Set P_{load} between 2 W to 13 W.
5. Measure V_{PSEPI_A} and V_{PSEPI_B}.
6. ↻ Repeat the test with pd_req_class set to 6, 7, and 8.

Pass requirements: For each test where class_event_count ≥ 4 both V_{PSEPI_A} and V_{PSEPI_B} must be in the range of $\Updownarrow V_{Port\_PSE\text{-}2P}$ for the given PSE Type.

PSE Type	Type 3	Type 4
$\Updownarrow V_{Port\_PSE\text{-}2P}$ (V)	50 – 57	52 – 57

9.61 PSE61 Output voltage during transients from 30 µs to 250 µs

This test is for PICS PSE61, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.3.

Requirement from IEEE Std 802.3bt™-2018

A PSE shall maintain an output voltage no less than $V_{Tran\text{-}2P}$ for transient conditions lasting more than 30 µs and less than 250 µs, and meet the requirements of 145.2.10.8.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.62 PSE62 Output voltage during transients longer than 250 µs

This test is for PICS PSE62, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.3.

Requirement from IEEE Std 802.3bt™-2018
Transients lasting more than 250 µs shall meet the $V_{Port\_PSE\text{-}2P}$ specification.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.63 PSE63 Reverse negative pair current

This test is for PICS PSE63, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.4.

Requirement from IEEE Std 802.3bt™-2018

The PSE shall not source a current higher than I_{rev}, as defined in Table 145–16, on a negative pair. This requirement holds only when no power is being sourced into the PSE.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.64 PSE64 Output voltage noise

This test is for PICS PSE64, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.5.

Requirement from IEEE Std 802.3bt™-2018

V_{Noise}, the specification for power feeding ripple and noise in Table 145–16, shall be met for common-mode and pair-to-pair noise values at all static PSE output voltages.

Last modification: Version 1.1.

History of changes:

Version 1.1 Added a high pass filter to the measurement circuit in Figure 9 to make the test insensitive to PD load changes, as well as fixed the PI pin numbering.

Test setup: Connect the SSPD model to the PSE with the following modifications:

- Disable Ethernet capability of the SSPD model
- Connect the measurement circuit shown in Figure 9 to the PI of the PSE (in parallel to the connection to the SSPD model). The impedance of the voltage meters must be such that the detection signature of the SSPD model remains valid when this is called for.
- pd_req_class set to 8

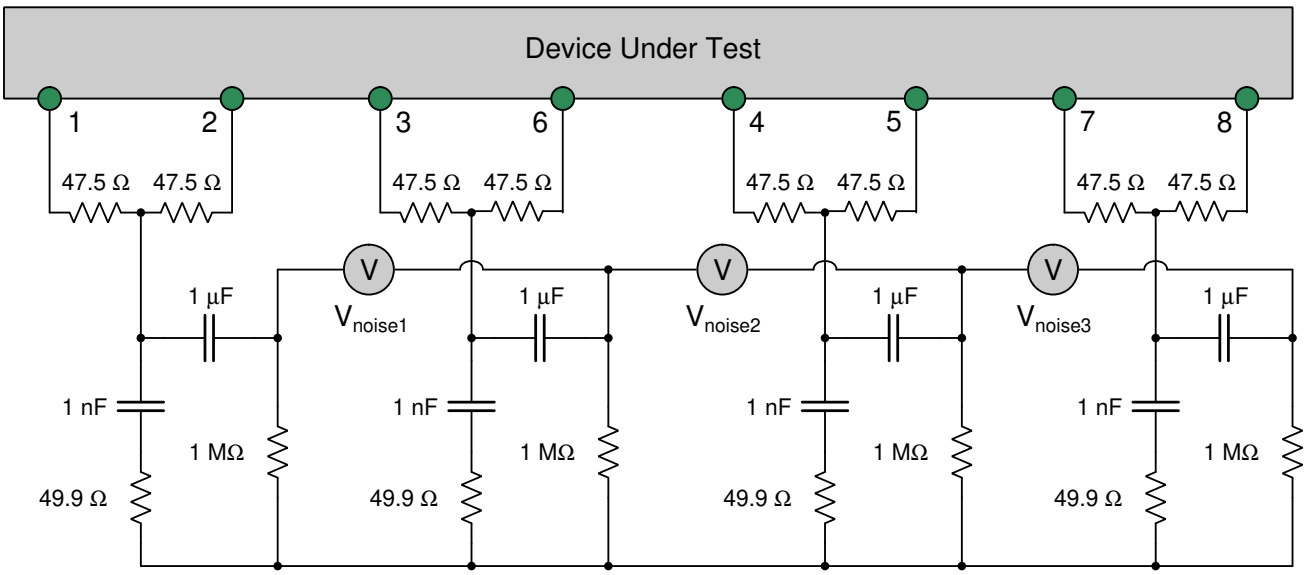

Figure 9: Pair-to-pair voltage noise measurement circuit

Test procedure:

1. Enable the PSE and wait for the PD to be powered up.
2. Set $\Diamond P_{load}$ between 90% and 100% of $\Diamond P_{Class\_PD}$ per pse_assigned_class.
3. Measure the voltage peak amplitude at V_{noise1}, V_{noise2}, and V_{noise3} (see Figure 9) with the measurement set to a bandlimited sampling of 2 kHz over the following frequency bands:
   - less than 0.5 kHz

- 0.5 kHz to 150 kHz
- 150 kHz to 500 kHz
- 500 kHz to 1000 kHz

4. Let $V_{ppn} = V_{noisen} \cdot 2\sqrt{2}$
5. Repeat the test with pd_req_class set to 6, 4, and 3

Assigned Class	1	2	3	4	5	6	7	8
$\Rightarrow P_{Class\_PD}$ (W)	3.84	6.49	13	25.5	40	51	62	71.3

Pass requirements: The measured peak-to-peak voltage does not exceed $\Rightarrow V_{noise}$:

- 0.5 V_{pp} for frequencies less than 0.5 kHz
- 0.2 V_{pp} for frequencies from 0.5 kHz to 150 kHz
- 0.15 V_{pp} for frequencies from 150 kHz to 500 kHz
- 0.1 V_{pp} for frequencies from 500 kHz to 1000 kHz

9.65 PSE65 Support $I_{Con\text{-}2P}$ on each powered pair

This test is for PICS PSE65, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.6.

> Requirement from IEEE Std 802.3bt™-2018
>
> PSEs shall be able to supply $I_{Con\text{-}2P}$, the current the PSE supports on both pairs of each powered pairset, as defined in Equation (145–8).

Last modification: Initial version.

History of changes: —

9.65.1 Test 1 — support total output power, single-signature

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to 1 and with (R_{pair1}, R_{pair2}, R_{pair3}, and R_{pair4}) in the range of 5 Ω to 6.25 Ω. Note that the requirements in Section 5.1 regarding the connection between the DUT and the test fixture apply.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Adjust P_{load} such that $V_{SSPD} \times I_{PD} = ⇳P_{Class\_PD}$ for the assigned Class.
3. Confirm the PSE maintains power.
4. ↻ Repeat the test with pd_req_class set to 2, 3, 4, 5, 6, 7, and 8.

Assigned Class	1	2	3	4	5	6	7	8
$⇳P_{Class\_PD}$ (W)	3.84	6.49	13	25.5	40	51	62	71.3

Pass requirements: PSE maintains power. If the PSE has a maximum power capability of Class 1 or Class 2, it will not turn on the PD when pd_req_class is set higher than what it can support. That does not constitute a failure.

9.65.2 Test 2 — support total output power, single-signature, forced 100% unbalance

Test setup: Connect the SSPD model to the PSE with pd_req_class set to 1 and with (R_{pair1}, R_{pair2}, R_{pair3}, and R_{pair4}) in the range of 5 Ω to 6.25 Ω. Note that the requirements in Section 5.1 regarding the connection between the DUT and the test fixture apply.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Measure V_{PSEPI_A} and V_{PSEPI_B}.
3. If both V_{PSEPI_A} and V_{PSEPI_B} are greater than 50 V proceed with the next step, otherwise go to step 10.
4. Adjust P_{load} such that $V_{SSPD} \times I_{PD} = ⇳P_{Class\_PD}$ for the assigned Class.

5. Disconnect pair 3 and pair 4 from the PSE (or set R_{pair3} and $R_{pair4} \geq 1\,k\Omega$).
6. Confirm the PSE maintains power.
7. Reconnect pair 3 and pair 4.
8. Disconnect pair 1 and pair 2 from the PSE (or set R_{pair1} and $R_{pair2} \geq 1\,k\Omega$).
9. Confirm the PSE maintains power.
10. ↻ Repeat the test with pd_req_class set to 2, 3, and 4, and with all pairs reconnected.

Assigned Class	1	2	3	4	5	6	7	8
⇩P_{Class_PD} (W)	3.84	6.49	13	25.5	40	51	62	71.3

NOTE — If the SSPD is capable of switching input current off on a per-pair basis, this may also be used to "disconnect pairs" for steps 5 and 8.

Pass requirements: PSE maintains power. If the PSE has a maximum power capability of Class 1 or Class 2, it will not turn on the PD when pd_req_class is set higher than what it can support. That does not constitute a failure. If a PSE does not provide power in 4-pair mode then this unbalance test cannot be performed. This is checked in step 3.

9.65.3 Test 3 — support output power for each Alternative, dual-signature

Test setup: Connect the DSPD model to the PSE with pd_req_class_modeA and pd_req_class_modeB set to permutation 1 in Table 35 and with (R_{pair1}, R_{pair2}, R_{pair3}, and R_{pair4}) in the range of 5 Ω to 6.25 Ω. Note that the requirements in Section 5.1 regarding the connection between the DUT and the test fixture apply.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Adjust P_{loadA} such that $V_{DSPD\_A} \times I_{PDA} = ⇩P_{Class\_PD\text{-}2P}$ for the assigned Class on Alternative A (if Alternative A is turned on by the PSE).
3. Adjust P_{loadB} such that $V_{DSPD\_B} \times I_{PDB} = ⇩P_{Class\_PD\text{-}2P}$ for the assigned Class on Alternative B (if Alternative B is turned on by the PSE).
4. Confirm that the PSE maintains power on the Alternatives that were turned on after step 1.
5. ↻ Repeat the test for each permutation in Table 35.

Assigned Class	1	2	3	4	5
⇩$P_{Class\_PD\text{-}2P}$ (W)	3.84	6.49	13	25.5	35.6

Table 35: Class permutations for PSE65

Permutation	pd_req_class_modeA	pd_req_class_modeB
1	1	5
2	5	1
3	3	4
4	4	2
5	5	5
6	3	3
7	4	4

Pass requirements: PSE maintains power on each Alternative that is initially powered after turning on the PSE. If the PSE has a maximum power capability of Class 1 or Class 2 on a given Alternative, it will not turn on the PD when pd_req_class_modeA or pd_req_class_modeB is set higher than what it can support. That does not constitute a failure.

9.65.4 Test 4 — support $I_{Con\text{-}2P\text{-}unb}$, single-signature

Test applicable to: PSE Logo Class 5 or greater

Test setup: Connect the SSPD model to the PSE with pd_req_class set to 5.

Test procedure:

1. Enable the PSE.
2. Perform a classification waveform measurement.
3. Wait for the PD test fixture to be powered up.
4. If the assigned Class is 4 or less (class_event_count ≤ 3), skip to step 11.
5. Disconnect pair 3 and pair 4 from the PSE (or set R_{pair3} and $R_{pair4} \geq 1\,k\Omega$).
6. Set P_{load} such that $I_{PD} = \Rightarrow I_{Con\text{-}2P\text{-}unb}$ for the assigned Class.
7. Confirm that power is maintained.
8. Reconnect pair 3 and pair 4.
9. Disconnect pair 1 and pair 2 from the PSE (or set R_{pair1} and $R_{pair2} \geq 1\,k\Omega$).
10. Confirm that power is maintained.
11. ↻ Repeat the test with pd_req_class set to 6, 7, and 8, and with all pairs reconnected.

Assigned Class	5	6	7	8
$\Rightarrow I_{Con\text{-}2P\text{-}unb}$ (mA)	560	692	794	948

NOTE — If the SSPD is capable of switching input current off on a per-pair basis, this may also be used to "disconnect pairs" for steps 5 and 9.

Pass requirements: The PSE maintains power.

9.66 PSE66 Support $I_{Peak\text{-}2P}$ on each powered pair

This test is for PICS PSE66, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.6.

> Requirement from IEEE Std 802.3bt™-2018
>
> The PSE shall support the AC current waveform parameter $I_{Peak\text{-}2P}$, defined in Equation (145–10), on both pairs of each powered pairset, while within the operating voltage range of $V_{Port\_PSE\text{-}2P}$, for a minimum of T_{CUT} and a duty cycle of at least 5%.

Last modification: Initial version.

History of changes: —

9.66.1 Test 1 — support total peak output power, single-signature

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to 1 and with (R_{pair1}, R_{pair2}, R_{pair3}, and R_{pair4}) in the range of 5 Ω to 6.25 Ω. Note that the requirements in Section 5.1 regarding the connection between the DUT and the test fixture apply.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Set P_{load} such that $V_{SSPD} \times I_{PD} = \Rightarrow P_{Class\_PD} - 0.2\,W$ for the assigned Class.
3. Set P_{load} such that $V_{SSPD} \times I_{PD}$ is in the range of $\Rightarrow P_{Peak\_PD} - 0.25\,W$ to $\Rightarrow P_{Peak\_PD}$ for no more than 50 ms within any period of 1 s (on top of the DC power value set previously).
4. Confirm the PSE maintains power.
5. ↻ Repeat the test with pd_req_class set to 2, 3, 4, 5, 6, 7, and 8.

Assigned Class	1	2	3	4	5	6	7	8
$\Rightarrow P_{Class\_PD}$ (W)	3.84	6.49	13	25.5	40	51	62	71.3
$\Rightarrow P_{Peak\_PD}$ (W)	5	8.36	14.4	28.3	42	53.5	65.1	74.9

Pass requirements: PSE maintains power. If the PSE has a maximum power capability of Class 1 or Class 2, it will not turn on the PD when pd_req_class is set higher than what it can support. That does not constitute a failure.

9.66.2 Test 2 — support total peak output power, single-signature, forced 100% unbalance

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to 1 and with (R_{pair1}, R_{pair2}, R_{pair3}, and R_{pair4}) in the range of 5 Ω to 6.25 Ω. Note that the requirements in Section 5.1 regarding the connection between the DUT and the test fixture apply.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Set P_{load} such that $V_{SSPD} \times I_{PD} = \Rightarrow P_{Class\_PD} - 0.2\,W$ for the assigned Class.
3. Set P_{load} such that $V_{SSPD} \times I_{PD}$ is in the range of $\Rightarrow P_{Peak\_PD} - 0.25\,W$ to $\Rightarrow P_{Peak\_PD}$ for no more than 50 ms within any period of 1 s (on top of the DC power value set previously).
4. Disconnect pair 3 and pair 4 from the PSE (or set R_{pair3} and $R_{pair4} \geq 1\,k\Omega$).
5. Confirm the PSE maintains power.
6. Reconnect pair 3 and pair 4.
7. Disconnect pair 1 and pair 2 from the PSE (or set R_{pair1} and $R_{pair2} \geq 1\,k\Omega$).
8. Confirm the PSE maintains power.
9. ↻ Repeat the test with pd_req_class set to 2, 3, and 4, and with all pairs reconnected.

Assigned Class	1	2	3	4	5	6	7	8
$\Rightarrow P_{Class\_PD}$ (W)	3.84	6.49	13	25.5	40	51	62	71.3
$\Rightarrow P_{Peak\_PD}$ (W)	5	8.36	14.4	28.3	42	53.5	65.1	74.9

NOTE — If the SSPD is capable of switching input current off on a per-pair basis, this may also be used to "disconnect pairs" for steps 4 and 7.

Pass requirements: PSE maintains power. If the PSE has a maximum power capability of Class 1 or Class 2, it will not turn on the PD when pd_req_class is set higher than what it can support. That does not constitute a failure.

9.66.3 Test 3 — support peak output power for each Alternative, dual-signature

Test applicable to: PSE Logo Class 5 and greater.

Test setup: Connect the DSPD model to the PSE with pd_req_class_modeA and pd_req_class_modeB set to permutation 1 in Table 35 and with (R_{pair1}, R_{pair2}, R_{pair3}, and R_{pair4}) in the range of 5 Ω to 6.25 Ω. Note that the requirements in Section 5.1 regarding the connection between the DUT and the test fixture apply.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Set P_{loadA} such that $V_{DSPD\_A} \times I_{PDA} = \Rightarrow P_{Class\_PD\text{-}2P}$ for the assigned Class on Alternative A (if Alternative A is turned on by the PSE).
3. Set P_{loadB} such that $V_{DSPD\_B} \times I_{PDB} = \Rightarrow P_{Class\_PD\text{-}2P}$ for the assigned Class on Alternative B (if Alternative B is turned on by the PSE).
4. Set P_{loadA} such that $V_{DSPD\_A} \times I_{PDA}$ is in the range of $\Rightarrow P_{Peak\_PD\text{-}2P} - 0.25\,W$ to $\Rightarrow P_{Peak\_PD\text{-}2P}$, for the assigned Class on Mode A, for no more than 50 ms within any period of 1 s (on top of the DC power value set previously).
5. Set P_{loadB} such that $V_{DSPD\_B} \times I_{PDB} = \Rightarrow P_{Peak\_PD\text{-}2P}$, for the assigned Class on Mode B, for no more than 50 ms within any period of 1 s (on top of the DC power value set previously). The accuracy for this P_{load} setting needs to be better than 0.25 W.

6. Confirm that the PSE maintains power on the Alternatives that were turned on after step 1.
7. ↻ Repeat the test for each permutation in Table 35.

Assigned Class	1	2	3	4	5
⇩$P_{Class\_PD\text{-}2P}$ (W)	3.84	6.49	13	25.5	35.6
⇩$P_{Peak\_PD\text{-}2P}$ (W)	5	8.36	14.4	28.3	37.4

Pass requirements: PSE maintains power on each Alternative that is initially powered after turning on the PSE. If the PSE has a maximum power capability of Class 1 or Class 2 on a given Alternative, it will not turn on the PD when pd_req_class_modeA or pd_req_class_modeB is set higher than what it can support. That does not constitute a failure.

9.66.4 Test 4 — support $I_{Peak\text{-}2P\text{-}unb}$, single-signature

Test applicable to: PSE Logo Class 5 and greater.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to 5.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. If the assigned Class is 4 or less, skip to step 10.
3. Disconnect pair 3 and pair 4 from the PSE (or set R_{pair3} and $R_{pair4} \geq 1\,k\Omega$).
4. Set P_{load} such that $I_{PD} = ⇩I_{Con\text{-}2P\text{-}unb}$ for the assigned Class.
5. Set P_{load} such that $I_{PD} = ⇩I_{Peak\text{-}2P\text{-}unb}$, for no more than 50 ms within any period of 1 s (on top of the DC power value set previously). The accuracy for this P_{load} setting needs to be better than 0.25 W.
6. Confirm that power is maintained.
7. Reconnect pair 3 and pair 4.
8. Disconnect pair 1 and pair 2 from the PSE (or set R_{pair1} and $R_{pair2} \geq 1\,k\Omega$).
9. Confirm that power is maintained.
10. ↻ Repeat the test with pd_req_class set to 6, 7, and 8, and with all pairs reconnected.

Assigned Class	5	6	7	8
⇩$I_{Con\text{-}2P\text{-}unb}$ (mA)	560	692	794	948
⇩$I_{Peak\text{-}2P\text{-}unb}$ (mA)	578	718	848	1.003

NOTE — If the SSPD is capable of switching input current on a per-pair basis, this may also be used to “disconnect pairs” for steps 3 and 8.

Pass requirements: The PSE maintains power.

9.67 PSE67 PSE unbalance contribution

This test is for PICS PSE67, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.10.6.1.

Requirement from IEEE Std 802.3bt™-2018

A PSE shall not source more than $I_{Unbalance\text{-}2P}$ on any pair when connected to a load as shown in Figure 145–21, using values of R_{load_min} and R_{load_max} as defined in Equation (145–14) and Equation (145–15).

Last modification: Initial version.

History of changes: —

Test applicable to: PSE Logo Class 5 and greater.

Test setup:

- Connect the SSPD model to the PSE with pd_req_class set to 5
- Set the resistance of the connection between the PSE and the test fixture (Figure 2) as follows:
  - Pair 1 & Pair 3: 5.47 Ω ±1%
  - Pair 2 & Pair 4: 6.18 Ω ±1%

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. If the assigned Class is less than Class 5, skip to step to step 5.
3. Set P_{load} such that $V_{SSPD} \times I_{PD} = ⇳P_{Class\_PD}$.
4. Measure I_{pair1}, I_{pair2}, I_{pair3}, and I_{pair4}.
5. ↻ Repeat the test with pd_req_class set to 6, 7, and 8.

Assigned Class	1	2	3	4	5	6	7	8
$⇳P_{Class\_PD}$ (W)	3.84	6.49	13	25.5	40	51	62	71.3

Pass requirements: I_{pair1}, I_{pair2}, I_{pair3}, and I_{pair4} are less than $⇳I_{Unbalance\text{-}2P}$ for the assigned Class.

Assigned Class	5	6	7	8
$⇳I_{Unbalance\text{-}2P}$ (mA)	550	682	784	938

9.68 PSE68 Complete power up

This test is for PICS PSE68, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.7.

> Requirement from IEEE Std 802.3bt™-2018
>
> A PSE that provides current on both pairsets during POWER_UP shall complete power up within T_{Inrush} max, starting when the first pairset exceeds a voltage of 30 V.

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to 4

Test procedure: Let t_0 be the time where V_{PSEPI_A} or V_{PSEPI_B} exceeds 30 V.

1. Enable the PSE.
2. At $t_0 + 75$ ms set P_{load} such that $V_{SSPD} \times I_{PD} = \Rightarrow P_{Class\_PD}$.
3. Confirm that V_{PSEPI} is in the range of $\Rightarrow V_{Port\_PSE\text{-}2P}$ between $t_0 + 75$ ms and $t_0 + 200$ ms.
4. ↻ Repeat the test with pd_req_class set to 5 and 7.

Pass requirements: V_{PSEPI} remains in the $\Rightarrow V_{Port\_PSE\text{-}2P}$ range during the time period noted in step 3 and the PSE does not turn off the power.

PSE Type	Type 3	Type 4
$\Rightarrow V_{Port\_PSE\text{-}2P}$ (V)	50 – 57	52 – 57

9.69 PSE69 $I_{Inrush\text{-}2P}$ and I_{Inrush} limits during power up

This test is for PICS PSE69, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.7.

> Requirement from IEEE Std 802.3bt™-2018
>
> The PSE shall limit the current on each powered negative pair to $I_{Inrush\text{-}2P}$ and the total current on the negative pairs to I_{Inrush} during power up per the requirements of Table 145–16, with the exception of the initial per pairset transient described in Equation (145–16).

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to 4. The behavior is modified to bypass the SSPD inrush limiter as follows:

Table 36: SSPD behavior modification for PSE69

PD State diagram variable			SSPD model element
pd_max_power			
	inrush	⇒	S_2 = closed, $I_{inrushlim}$ = 0 mA

Test procedure: Let t_0 be the time where V_{PSEPI} exceeds 30 V.

1. Measure V_{PSEPI}, I_{PDA} and I_{PDB} continuously.
2. Enable the PSE and wait for the PD to be turned on.
3. ↻ Repeat the test with pd_req_class set to 5 and 7.

Pass requirements: During each test:

- I_{PDA} and I_{PDB} never exceed 50 A
- I_{PDA} and I_{PDB} are less than ⇩$I_{Inrush\text{-}2P}$ between $t_0 + 1$ ms and $t_0 + 75$ ms

Assigned Class	1 to 4	5 to 8
⇩$I_{Inrush\text{-}2P}$ (single-signature) (mA)	450	600

9.70 PSE70 I_{Inrush} and $I_{Inrush\text{-}2P}$ when V_{PSE} is less than 30 V

This test is for PICS PSE70, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.7.

Requirement from IEEE Std 802.3bt™-2018

During a power up state, the PSE shall support:

— when powering a single-signature PD, a minimum I_{Inrush} of 5 mA when V_{PSE} is between 0 V and 10 V, and 60 mA when V_{PSE} is between 10 V and 30 V,

— when powering a dual-signature PD, a minimum $I_{Inrush\text{-}2P}$ of 5 mA when V_{PSE} is between 0 V and 10 V, and 60 mA when V_{PSE} is between 10 V and 30 V.

Last modification: Initial version.

History of changes: —

9.70.1 Test 1 — Single-signature PD

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with a voltage limiting element placed in parallel with C_{bulk}.

Test procedure:

1. Disable the voltage limiting element.
2. Enable the PSE.
3. Wait until $t_{classification\_end}$ and mark this time as t_0.
4. At t_0, set the voltage limiting element (in parallel with C_{bulk}) to 6 V.
5. Measure I_{PD} from t_0 to $t_0 + 50$ ms..
6. Disconnect the SSPD.
7. Disable the voltage limiting element.
8. Reconnect the SSPD.
9. Wait for $t_{classification\_end}$ and mark this time as t_1.
10. At t_1, set the voltage limiting element (in parallel with C_{bulk}) to 20 V.
11. Measure I_{PD} from t_1 to $t_1 + 50$ ms.

Pass requirements: The measured I_{PD} exceeds 5 mA in step 5 and exceeds 60 mA in step 11.

9.70.2 Test 2 — Dual-signature PD

Test applicable to: PSE Logo Class 5 and greater.

Test setup: Connect the DSPD model to the PSE with a voltage limiting element placed in parallel with C_{bulkA} and C_{bulkB}.

Test procedure:

1. Disable both voltage limiting elements.
2. Enable the PSE.
3. Wait for $t_{classification\_endA}$ and $t_{classification\_endB}$ and mark these times as t_0 and t_1 respectively.
4. At t_0, set the voltage limiting element (in parallel with C_{bulkA}) to 6 V.
5. At t_1, set the voltage limiting element (in parallel with C_{bulkB}) to 6 V.
6. Measure I_{PDA} from t_0 to $t_0 + 50$ ms.
7. Measure I_{PDB} from t_1 to $t_1 + 50$ ms.
8. Disconnect the DSPD.
9. Disable both voltage limiting elements.
10. Reconnect the DSPD.
11. Wait for $t_{classification\_endA}$ and $t_{classification\_endB}$ and mark these times as t_2 and t_3 respectively.
12. At t_2, set the voltage limiting element (in parallel with C_{bulkA}) to 20 V.
13. At t_3, set the voltage limiting element (in parallel with C_{bulkB}) to 20 V.
14. Measure I_{PDA} from t_2 to $t_2 + 50$ ms.
15. Measure I_{PDB} from t_3 to $t_3 + 50$ ms.

Pass requirements: The measured I_{PDA} and I_{PDB} exceed 5 mA in step 6 and 7 and exceed 60 mA in step 14 and 15.

9.71 PSE71 Pairset current limiting

This test is for PICS PSE71, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.9.

Requirement from IEEE Std 802.3bt™-2018

The PSE shall limit the pairset current to $I_{LIM\text{-}2P}$ for a duration of at least T_{LIM} min when V_{PSE} is in the range of $V_{Port\_PSE\text{-}2P}$.

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to the PSE Logo Class.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Set P_{load} such that $I_{PD} > 10A$ and mark the time as t_0.
   NOTE—The current will be limited by the PSE, so should not reach this level.
3. Measure I_{PDA} and I_{PDB} from t_0 to 75 ms [$\Rightarrow T_{CUT}$ max].

Pass requirements:

- For time $t_0 + 1$ ms to $t_0 + 3$ ms: $I_{PDA} < 5A$ and $I_{PDB} < 5A$
- For time $t_0 + 3$ ms to $t_0 + 10$ ms: $I_{PDA} < 3A$ and $I_{PDB} < 3A$
- For time $t_0 + 10$ ms to $t_0 + 75$ ms: $I_{PDA} < 1.75A$ and $I_{PDB} < 1.75A$

9.72 PSE72 Power removal when current limit persists

This test is for PICS PSE72, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.9.

Requirement from IEEE Std 802.3bt™-2018
The PSE shall remove power from a pairset before a current limit event persists on that pairset continuously for T_{LIM} max as defined in Table 145–16.

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Increase P_{load} until I_{PD} no longer increases (PSE is limiting the current).
3. Mark the time where I_{PD} no longer increases as t_0.
4. Wait until power is removed or 5 s have passed.

Pass requirements: Power is removed no later than $t_0 + 75\,ms$[⇩T_{CUT} max].

9.73 PSE73 Upperbound template

This test is for PICS PSE73, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.9.

Requirement from IEEE Std 802.3bt™-2018
Power shall be removed from a pairset of a PSE before the pairset current exceeds the 'PSE upperbound template' in Figure 145–23 or Figure 145–24.

Last modification: Initial version.

History of changes: —

9.73.1 Test 1 — Type 3, SSPD model

Test applicable to: Type 3 PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to the PSE Logo Class.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Set P_{load} such that $I_{PD} \geq 1.75A$ and mark the time as t_0.

Pass requirements: The PSE turns off power to the port no later than $t_0 + 150\,ms$.

9.73.2 Test 2 — Type 3, DSPD model

Test applicable to: Type 3 PSE with PSE Logo Class 5 or 6.

Test setup: Connect the DSPD model to the PSE with pd_req_class_modeA and pd_req_class_modeB set to the corresponding value per the PSE Logo Class (see Table 2).

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Set P_{loadA} such that $I_{PDA} \geq 0.9A$ and mark the time as t_0 (note: P_{loadB} is at the default value defined in Table 12).
3. ↻ Repeat the test, with the power settings for P_{loadA} and P_{loadB} exchanged.
4. ↻ Repeat the test, with both P_{loadA} and P_{loadB} set such that I_{PDA} and $I_{PDB} \geq 0.9\,A$.

Pass requirements:

The PSE turns off power to the pairset with the overload no later than $t_0 + 75\,ms[\Diamond T_{CUT}$ max].

9.73.3 Test 3 — Type 4, SSPD model

Test applicable to: Type 4 PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to PSE Logo Class.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Set P_{load} such that $I_{PD} \geq 2.65A$ and mark the time as t_0.

Pass requirements: The PSE turns off power to the port no later than $t_0 + 150\,ms$.

9.73.4 Test 4 — Type 4, DSPD model

Test applicable to: Type 4 PSEs.

Test setup: Connect the DSPD model to the PSE with pd_req_class_modeA and pd_req_class_modeB set according to Table 2 according to the PSE Logo Class.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Set P_{loadA} such that $I_{PDA} \geq 1.35A$ and mark the time as t_0 (note: P_{loadB} is at the default value defined in Table 12).
3. ↻ Repeat the test, with the power settings for P_{loadA} and P_{loadB} exchanged.
4. ↻ Repeat the test, with both P_{loadA} and P_{loadB} set such that I_{PDA} and $I_{PDB} \geq 1.35\,A$.

Pass requirements:

The PSE turns off power to the pairset with the overload no later than $t_0 + 75\,ms[\Diamond T_{CUT}$ max].

9.74 PSE74 Turn off time

This test is for PICS PSE74, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.9.

> Requirement from IEEE Std 802.3bt™-2018
>
> The specification for T_{Off} in Table 145–16 shall apply to the discharge time from $V_{Port\_PSE\text{-}2P}$ min to V_{Off} of a pairset with a test resistor of 320 kΩ attached to that pairset.

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connect the DSPD model to the PSE.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Close S_{1A} and S_{1B}, set R_{detA} and R_{detB} to a value of 320 kΩ.
3. For each mode that is powered set P_{loadA} or P_{loadB} to 0 W, such that the DSPD no longer provides a DC MPS signature.
4. Measure V_{PSEPI_A} and V_{PSEPI_B} continuously.
5. When V_{PSEPI_A} falls below $\Rightarrow V_{Port\_PSE\text{-}2P}$ min, mark the time as t_0.
6. When V_{PSEPI_B} falls below $\Rightarrow V_{Port\_PSE\text{-}2P}$ min, mark the time as t_1.
7. When V_{PSEPI_A} falls below 2.8 V [$\Rightarrow V_{Off}$], mark the time as t_2.
8. When V_{PSEPI_B} falls below 2.8 V [$\Rightarrow V_{Off}$], mark the time as t_3.

PSE Type	Type 3	Type 4
$\Rightarrow V_{Port\_PSE\text{-}2P}$ min (V)	50	52

Pass requirements: The PSE must turn off such that $t_2 - t_0 \leq 500$ ms[$\Rightarrow T_{Off}$] and $t_3 - t_1 \leq 500$ ms[$\Rightarrow T_{Off}$].

9.75 PSE75 PI voltage when idle

This test is for PICS PSE75, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.11.

> Requirement from IEEE Std 802.3bt™-2018
>
> The voltage at the PI shall be equal or less than V_{Off}, as defined in Table 145–16, when the PSE is in DISABLED, IDLE, BACKOFF, or ERROR_DELAY.

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

9.75.1 Test 1 — Between detection

Test setup: Connect the SSPD model to the PSE with the following modification:

- An invalid detection signature is created by at least one of the following:
  - R_{det} is set higher than 33 kΩ [⇩R_{bad} max] or set lower than 15 kΩ [⇩R_{bad} min]
  - C_{in} is set higher than 10 µF [⇩C_{bad}]

Test procedure:

1. Enable the PSE.
2. Measure V_{PSEPI} continuously for at least 2 s.

Pass requirements: V_{PSEPI} is less than 2.8 V [⇩V_{Off}] in any window with a width of at least 515 ms for at least 15 ms [⇩T_{Reset}] continuously.

9.75.2 Test 2 — After POWER_ON

Test setup: Connect the SSPD model to the PSE.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered on.
2. Set P_{load} to 0 W, such that the SSPD no longer provides a DC MPS signature.
3. Measure V_{PSEPI} and wait for the voltage to drop below 30 V.
4. Mark as t_0 the moment when V_{PSEPI} falls below 30 V.
5. Measure V_{PSEPI} continuously for at least 2 s.

Pass requirements: After t_0 V_{PSEPI} is less than 2.8 V [⇩V_{Off}] for at least 15 ms [⇩T_{Reset}] before V_{PSEPI} rises above 2.8 V [⇩V_{Off}].

9.75.3 Test 3 — After a fault (ERROR_DELAY)

Test setup: Connect the SSPD model to the PSE.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered on.
2. Set P_{load} to a value between 100 W to 150 W.
3. Measure V_{PSEPI} and wait for the voltage to drop below 30 V.
4. Mark as t_0 the moment when V_{PSEPI} falls below 30 V.
5. Measure V_{PSEPI} continuously for at least 2 s.

Pass requirements: After t_0 V_{PSEPI} is less than 2.8 V [⇩V_{Off}] for at least 15 ms [⇩T_{Reset}] before V_{PSEPI} rises above 2.8 V [⇩V_{Off}].

9.76 PSE76 Pairset voltage when idle

This test is for PICS PSE76, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.11.

> Requirement from IEEE Std 802.3bt™-2018
>
> The voltage at the corresponding pairset shall be equal or less than V_{Off}, as defined in Table 145–16, when the PSE is in IDLE_PRI, WAIT_PRI, ERROR_DELAY_PRI, IDLE_SEC, WAIT_SEC, or ERROR_DELAY_SEC.

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

9.76.1 Test 1 — between detection

Test setup: Connect the DSPD model to the PSE with the following modification:

- An invalid detection signature is created on Mode A by at least one of the following:
  - R_{detA} is set higher than 33 kΩ [⇳R_{bad} max] or set lower than 15 kΩ [⇳R_{bad} min]
  - C_{inA} is set higher than 10 µF [⇳C_{bad}]
- An invalid detection signature is created on Mode B by at least one of the following:
  - R_{detB} is set higher than 33 kΩ [⇳R_{bad} max] or set lower than 15 kΩ [⇳R_{bad} min]
  - C_{inB} is set higher than 10 µF [⇳C_{bad}]

Test procedure:

1. Enable the PSE.
2. Measure V_{PSEPI_A} and V_{PSEPI_B} continuously for 2 s.

Pass requirements: V_{PSEPI_A} and V_{PSEPI_B} are less than 2.8 V [⇳V_{Off}] in any window with a width of at least 515 ms for at least 15 ms [⇳T_{Reset}] continuously.

9.76.2 Test 2 — after POWER_ON

Test setup: Connect the DSPD model to the PSE.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Set P_{loadA} to 0 W, such that the DSPD no longer provides a DC MPS signature on Mode A.
   If the PSE has not powered Mode A, skip to step 5.
3. Measure V_{PSEPI_A} and wait for the voltage to drop below 30 V.
4. Measure V_{PSEPI_A} continuously for 2 s.
5. ↻ Repeat the test for P_{loadB} and V_{PSEPI_B}.

Pass requirements: V_{PSEPI_A} and V_{PSEPI_B} are less than 2.8 V [⇩V_{Off}] for at least 15 ms [⇩T_{Reset}] before V_{PSEPI_A} or V_{PSEPI_B} rises above 2.8 V [⇩V_{Off}].

9.77 PSE77 Supported intra-pair current unbalance

This test is for PICS PSE77, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.12.

Requirement from IEEE Std 802.3bt™-2018
The PSE shall support an intra-pair current unbalance of I_{unb}, as defined in Equation (145–21).

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.78 PSE78 Endpoint PSEs transmitting 100BASE-TX in the presence of ($I_{unb}/2$)

This test is for PICS PSE78, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.12.

Requirement from IEEE Std 802.3bt™-2018
A 100BASE-TX transmitter in a Type 3 or Type 4 Endpoint PSE shall meet the requirements of 25.4.5 in the presence of ($I_{unb}/2$).

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.79 PSE79 Type 4 PSE output power limit

This test is for PICS PSE79, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.13.

Requirement from IEEE Std 802.3bt™-2018

Type 4 PSEs shall not source more power than P_{Type} max, as defined in Table 145–16, measured using a sliding window with a width up to 4 seconds.

Last modification: Initial version.

History of changes: —

Test applicable to: Type 4 PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to the PSE Logo Class.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Set P_{load} to a value between 100 W to 105 W and mark the time as t_0.
3. Wait for the PSE to turn off the power, or 5 s, whichever is shorter.

Pass requirements: The PSE removes power between t_0 and $t_0 + 4$ s.

9.80 PSE80 Detection to POWER_ON time (single-signature)

This test is for PICS PSE80, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.14.

> Requirement from IEEE Std 802.3bt™-2018
>
> PSEs, when connected to a single-signature PD, shall reach POWER_ON within T_{pon} after completing detection on the last pairset.

Last modification: Initial version.

History of changes: —

9.80.1 Test 1 — Class 4 and below

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to Class 3 or the PSE Logo Class, whichever is less.

Test procedure:

1. Perform a classification waveform measurement.
2. Enable the PSE and wait for the PD test fixture to be powered up.

Pass requirements: $(t_{classification\_end} - t_{classification\_start}) < 400\,ms[\Rightarrow T_{pon}]$.

9.80.2 Test 2 — Class 5 and higher

Test applicable to: PSE Logo Class 5 and greater.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to Class 5.

Test procedure:

1. Perform a classification waveform measurement.
2. Enable the PSE and wait for the PD test fixture to be powered up.
3. If the assigned Class is less than 5 (class_event_count < 4), this test is skipped.
4. Measure V_{PSEPI_A} and V_{PSEPI_B}.

Pass requirements:

- $(t_{classification\_end} - t_{classification\_start}) < \Rightarrow T_{pon}$
- Both V_{PSEPI_A} and V_{PSEPI_B} are in the range of $\Rightarrow V_{Port\_PSE\text{-}2P}$

PSE Type	Type 3	Type 4
$\Rightarrow V_{Port\_PSE\text{-}2P}$ (V)	50 – 57	52 – 57

9.81 PSE81 Detection to POWER_ON time per pairset (dual-signature)

This test is for PICS PSE81, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.10.14.

> Requirement from IEEE Std 802.3bt™-2018
>
> When connected to a dual-signature PD, PSEs shall reach the respective power on state for a pairset within T_{pon} after completing detection on the same pairset.

Last modification: Initial version.

History of changes: —

Test applicable to: PSE Logo Class 5 and greater.

Test setup: Connect the DSPD model to the PSE.

Test procedure:

1. Measure V_{PSEPI_A} and V_{PSEPI_B} continuously.
2. Mark the time when $V_{PSEPI\_A} > 10\,V$[⇨V_{valid} max] for the first time after enabling the PSE as t_0.
3. Mark the time when $V_{PSEPI\_B} > 10\,V$[⇨V_{valid} max] for the first time after enabling the PSE as t_1.
4. Mark the time when $V_{PSEPI\_A} > 30\,V$ for the first time after enabling the PSE as t_2.
5. Mark the time when $V_{PSEPI\_B} > 30\,V$ for the first time after enabling the PSE as t_3.
6. Enable the PSE and wait for the PD test fixture to be powered up.

Pass requirements:

- If Mode A is powered up: $(t_2 - t_0) < 400\,ms$[⇨T_{pon}]
- If Mode B is powered up: $(t_3 - t_1) < 400\,ms$[⇨T_{pon}]

9.82 PSE82 Power allocation

This test is for PICS PSE82, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.11.

> Requirement from IEEE Std 802.3bt™-2018
>
> Allocating power based on additional information about the attached PD, and the mechanism for obtaining that additional information, is beyond the scope of this standard with the exception that the allocation of power shall not be based solely on the historical data of the power consumption of the attached PD.

Last modification: Initial version.

History of changes: —

Test setup: Connect the SSPD model to the PSE.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Set P_{load} to any value in the range of 1 W to $0.75 \times \Rightarrow P_{Class\_PD}$.
3. Wait for any amount of time longer than 1 s.
4. Set P_{load} to $\Rightarrow P_{Class\_PD}$.

Assigned Class	1	2	3	4	5	6	7	8
$\Rightarrow P_{Class\_PD}$ (W)	3.84	6.49	13	25.5	40	51	62	71.3

Pass requirements: PSE maintains power.

9.83 PSE83 MPS applicable parameters

This test is for PICS PSE83, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.12.

Requirement from IEEE Std 802.3bt™-2018
A PSE, depending on the PD assigned Class and PD signature configuration, shall use the applicable I_{Hold}, $I_{Hold\text{-}2P}$, T_{MPS} and T_{MPDO} values as defined in Table 145–16.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.84 PSE84 Consider DC MPS component present (2-pair)

This test is for PICS PSE84, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.12.

Requirement from IEEE Std 802.3bt™-2018
A PSE powering a PD over a single pairset: shall consider the DC MPS component to be present if $I_{Port\text{-}2P}$ is greater than or equal to $I_{Hold\text{-}2P}$ max continuously for a minimum of T_{MPS}

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.85 PSE85 Consider DC MPS component absent (2-pair)

This test is for PICS PSE85, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.12.

Requirement from IEEE Std 802.3bt™-2018
A PSE powering a PD over a single pairset: shall consider the DC MPS component to be absent if $I_{Port\text{-}2P}$ is less than or equal to $I_{Hold\text{-}2P}$ min

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.86 PSE86 Power removal (2-pair)

This test is for PICS PSE86, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.12.

Requirement from IEEE Std 802.3bt™-2018
A PSE powering a PD over a single pairset: shall remove power from the PI when DC MPS has been absent for a duration greater than T_{MPDO}

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to 4.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Wait for at least 2 s and confirm power is maintained.
3. Measure V_{PDPI} continuously.
4. Set R_{det} to 320 kΩ.
5. Set P_{load} such that I_{PD} is less than 2 mA [⇩$I_{Hold\text{-}2P}$ min] and mark the time as t_0.

Pass requirements:

- $V_{PDPI} < 30$ V from $t_0 + 900$ ms until $t_0 + 1500$ ms
- $V_{PDPI} < 2.8$ V for at least 15 ms continuously anywhere between $t_0 + 400$ ms until $t_0 + 1000$ ms

9.87 PSE87 Maintain power (2-pair)

This test is for PICS PSE87, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.12.

Requirement from IEEE Std 802.3bt™-2018
A PSE powering a PD over a single pairset: shall not remove power from the PI when DC MPS has been present within the T_{MPS} + T_{MPDO} window.

Last modification: Initial version.

History of changes: —

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to 4.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Continuously measure V_{PSEPI}.
3. Set P_{load} to any value between 1 W and ⇩P_{Class_PD} and wait for at least 400 ms.
4. Mark the time as t_0.
5. Set P_{load} such that I_{PD} < 2 mA[⇩$I_{Hold\text{-}2P}$ min] and wait for 300 ms to 320 ms [⇩T_{MPDO} min].
6. Set P_{load} such that I_{PD} ≥ 9 mA[⇩$I_{Hold\text{-}2P}$ max] and wait for 6 ms [⇩T_{MPS}] to 8 ms.
7. Go back to step 5 and iterate until at least 5 s have passed since t_0.

NOTE—In step 6, make sure that the correct current level is present at the PSE PI.

Pass requirements: V_{PSEPI} is in the range of ⇩$V_{Port\_PSE\text{-}2P}$ from t_0 until the conclusion of the test.

PSE Type	Type 3	Type 4
⇩$V_{Port\_PSE\text{-}2P}$ (V)	50 – 57	52 – 57

9.88 PSE88 Consider DC MPS component present (4-pair, single-signature)

This test is for PICS PSE88, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.12.

Requirement from IEEE Std 802.3bt™-2018
A PSE powering a single-signature PD over both pairsets: shall consider the DC MPS component to be present if $I_{Port\text{-}2P}$ of the pairset with the highest current is greater than or equal to $I_{Hold\text{-}2P}$ max and I_{Port} is greater than or equal to I_{Hold} max continuously for a minimum of T_{MPS}

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.89 PSE89 Consider DC MPS component absent (4-pair, single-signature)

This test is for PICS PSE89, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.12.

Requirement from IEEE Std 802.3bt™-2018

A PSE powering a single-signature PD over both pairsets: shall consider the DC MPS component to be absent if $I_{Port\text{-}2P}$ of the pairset with the highest current is less than or equal to $I_{Hold\text{-}2P}$ min and I_{Port} is less than or equal to $I_{Holdmin}$

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.90 PSE90 Power removal (4-pair, single-signature)

This test is for PICS PSE90, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.12.

Requirement from IEEE Std 802.3bt™-2018
A PSE powering a single-signature PD over both pairsets: shall remove power from the PI when DC MPS has been absent for a duration greater than T_{MPDO}

Last modification: Initial version.

History of changes: —

9.90.1 Test 1 — Class 1 to 4

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to Class 4 or less.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Wait for at least 2 s and confirm power is maintained.
3. Measure V_{PDPI} continuously.
4. Set R_{det} to 320 kΩ.
5. Set P_{load} such that I_{PD} is less than 2 mA [⇩$I_{Hold\text{-}2P}$ min] and mark the time as t_0.

Pass requirements:

- $V_{PDPI} < 30$ V from $t_0 + 900$ ms until $t_0 + 1500$ ms
- $V_{PDPI} < 2.8$ V for at least 15 ms continuously anywhere between $t_0 + 400$ ms until $t_0 + 1000$ ms

9.90.2 Test 2 — Class 5 to 8

Test applicable to: PSE Logo Class 5 and greater.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to Class 5.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Confirm the PSE has assigned Class 5, otherwise the test is concluded.
3. Wait for at least 2 s and confirm power is maintained.
4. Measure V_{PDPI} continuously.
5. Set R_{det} to 320 kΩ.
6. Set P_{load} such that I_{PD} is less than 2 mA [⇩$I_{Hold\text{-}2P}$ min] and mark the time as t_0.

Pass requirements:

- $V_{PDPI} < 30\,V$ from $t_0 + 900\,ms$ until $t_0 + 1500\,ms$
- $V_{PDPI} < 2.8\,V$ for at least 15 ms continuously anywhere between $t_0 + 400\,ms$ until $t_0 + 1000\,ms$

9.91 PSE91 Maintain power (4-pair, single-signature)

This test is for PICS PSE91, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.12.

Requirement from IEEE Std 802.3bt™-2018
A PSE powering a single-signature PD over both pairsets: shall not remove power from the PI when DC MPS has been present within the T_{MPS} + T_{MPDO} window.

Last modification: Initial version.

History of changes: —

Test applicable to: 4-pair capable PSEs

9.91.1 Test 1 — Class 1 to 4

Test applicable to: All PSEs.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to 4 or less.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Continuously measure V_{PSEPI}.
3. Set P_{load} to any value between 1 W and ⇩P_{Class_PD} and wait for at least 400 ms.
4. Mark the time as t_0.
5. Set P_{load} such that I_{PD} < 2 mA[⇩$I_{Hold\text{-}2P}$ min] and wait for 300 ms to 320 ms [⇩T_{MPDO} min].
6. Set P_{load} such that I_{PD} ≥ 9 mA[⇩$I_{Hold\text{-}2P}$ max] and wait for 6 ms [⇩T_{MPS}] to 8 ms.
7. Go back to step 5 and iterate until at least 5 s have passed since t_0.

NOTE—In step 6, make sure that the correct current level is present at the PSE PI.

Pass requirements: V_{PSEPI} is in the range of ⇩$V_{Port\_PSE\text{-}2P}$ from t_0 until the conclusion of the test.

PSE Type	Type 3	Type 4
⇩$V_{Port\_PSE\text{-}2P}$ (V)	50 – 57	52 – 57

9.91.2 Test 2 — Class 5 to 8

Test applicable to: PSE Logo Class 5 and greater.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to 5.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Measure V_{PSEPI_A} and V_{PSEPI_B} continuously.
3. Confirm the PSE has assigned Class 5, otherwise the test is concluded.
4. Set P_{load} to any value between 1 W and ⇩P_{Class_PD} and wait for at least 400 ms.
5. Mark the time as t_0.
6. Set P_{load} such that $I_{PD} < 2$ mA[⇩$I_{Hold\text{-}2P}$ min] and wait for 300 ms to 320 ms [⇩T_{MPDO} min].
7. Set P_{load} such that $I_{PD} \geq 14$ mA[⇩I_{Hold} max] and wait for 6 ms [⇩T_{MPS}] to 8 ms.
8. Go back to step 6 and iterate until at least 5 s have passed since t_0.
9. Mark the time as t_1.
10. Disconnect pair 3 or pair 4 from the PSE, whichever is the negative pair (or set R_{pair3} or $R_{pair4} \geq 1$ kΩ).
11. Set P_{load} such that $I_{PD} < 2$ mA[⇩$I_{Hold\text{-}2P}$ min] and wait for 300 ms to 320 ms [⇩T_{MPDO} min].
12. Set P_{load} such that $I_{PD} \geq 14$ mA[⇩I_{Hold} max] and wait for 6 ms [⇩T_{MPS}] to 8 ms.
13. Go back to step 11 and iterate until at least 5 s have passed since t_1.
14. Mark the time as t_2.
15. Reconnect pair 3 and pair 4.
16. Disconnect pair 1 or pair 2 from the PSE, whichever is the negative pair (or set R_{pair1} or $R_{pair2} \geq 1$ kΩ).
17. Set P_{load} such that $I_{PD} < 2$ mA[⇩$I_{Hold\text{-}2P}$ min] and wait for 300 ms to 320 ms [⇩T_{MPDO} min].
18. Set P_{load} such that $I_{PD} \geq 14$ mA[⇩I_{Hold} max] and wait for 6 ms [⇩T_{MPS}] to 8 ms.
19. Go back to step 17 and iterate until at least 5 s have passed since t_2.

NOTE—In steps 7, 12, and 18 make sure that the correct current level is present at the PSE PI.

Pass requirements: V_{PSEPI_A} and V_{PSEPI_B} are both in the range of ⇩$V_{Port\_PSE\text{-}2P}$ from t_0 until the conclusion of the test.

PSE Type	Type 3	Type 4
⇩$V_{Port\_PSE\text{-}2P}$ (V)	50 – 57	52 – 57

9.92 PSE92 Dual-signature PD independent MPS

This test is for PICS PSE92, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.12.

Requirement from IEEE Std 802.3bt™-2018
A PSE powering a dual-signature PD over both pairsets: shall consider the DC MPS component to be present or absent on each pairset independently

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.93 PSE93 Consider DC MPS component present (4-pair, dual-signature)

This test is for PICS PSE93, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.12.

Requirement from IEEE Std 802.3bt™-2018

A PSE powering a dual-signature PD over both pairsets: shall consider the DC MPS component to be present on a pairset if $I_{Port\text{-}2P}$ is greater than or equal to $I_{Hold\text{-}2P}$ max continuously for a minimum of T_{MPS}

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.94 PSE94 Consider DC MPS component absent (4-pair, dual-signature)

This test is for PICS PSE94, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.12.

Requirement from IEEE Std 802.3bt™-2018
A PSE powering a dual-signature PD over both pairsets: shall consider the DC MPS component to be absent on a pairset if $I_{Port\text{-}2P}$ is less than or equal to $I_{Hold\text{-}2P}$ min

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

9.95 PSE95 Pairset power removal (4-pair, dual-signature)

This test is for PICS PSE95, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.12.

> Requirement from IEEE Std 802.3bt™-2018
>
> A PSE powering a dual-signature PD over both pairsets: shall remove power from a pairset when DC MPS has been absent on that pairset for a duration greater than T_{MPDO}

Last modification: Initial version.

History of changes: —

Test applicable to: PSE Logo Class 5 and greater.

9.95.1 Test 1 — Mode A

Test setup: Connect the DSPD model to the PSE.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Wait for at least 2 s and confirm power is maintained.
3. Measure V_{PDPI_A} continuously.
4. Set R_{detA} to 320 kΩ.
5. Set P_{loadA} such that I_{PDA} is less than 2 mA [$\Diamond I_{Hold\text{-}2P}$ min] and mark the time as t_0.

Pass requirements:

- $V_{PDPI\_A} < 30$ V from $t_0 + 900$ ms until $t_0 + 1500$ ms
- $V_{PDPI\_A} < 2.8$ V for at least 15 ms continuously anywhere between $t_0 + 400$ ms until $t_0 + 1000$ ms

9.95.2 Test 2 — Mode B

Test setup: Connect the DSPD model to the PSE.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up.
2. Wait for at least 2 s and confirm power is maintained.
3. Measure V_{PDPI_B} continuously.
4. Set R_{detB} to 320 kΩ.
5. Set P_{loadB} such that I_{PDB} is less than 2 mA [$\Diamond I_{Hold\text{-}2P}$ min] and mark the time as t_0.

Pass requirements:

- $V_{PDPI\_B} < 30$ V from $t_0 + 900$ ms until $t_0 + 1500$ ms
- $V_{PDPI\_B} < 2.8$ V for at least 15 ms continuously anywhere between $t_0 + 400$ ms until $t_0 + 1000$ ms

9.96 PSE96 Maintain power on pairset (4-pair, dual-signature)

This test is for PICS PSE96, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.2.12.

Requirement from IEEE Std 802.3bt™-2018
A PSE powering a dual-signature PD over both pairsets: shall not remove power from a pairset when DC MPS has been present on both pairsets within the T_{MPS} + T_{MPDO} window

Last modification: Initial version.

History of changes: —

Test applicable to: PSE Logo Class 5 and greater.

Test setup: Connect the DSPD model to the PSE.

Test procedure:

1. Enable the PSE and wait for it to apply operating power to both pairsets..
2. Measure V_{PSEPI_A} and V_{PSEPI_B} continuously.
3. Set P_{loadA} and P_{loadB} to any value between 1 W and ⇩$P_{Class\_PD\text{-}2P}$ and wait for at least 400 ms.
4. Mark the time as t_0.
5. Set P_{loadA} such that $I_{PDA} < 2$ mA[⇩$I_{Hold\text{-}2P}$ min] and wait for 300 ms to 320 ms [⇩T_{MPDO} min].
6. Set P_{loadA} such that $I_{PDA} \geq 7$ mA[⇩$I_{Hold\text{-}2P}$ max] and wait for 6 ms [⇩T_{MPS}] to 8 ms.
7. Concurrently run the same current pattern with P_{loadB} and I_{PDB}, this may be with different timings and may be out of sync with Mode A.
8. Go back to step 5 and iterate until at least 5 s have passed since t_0.

NOTE—In step 6, make sure that the correct current level is present at the PSE PI.

Pass requirements: V_{PSEPI_A} and V_{PSEPI_B} (whichever were turned on in step 1) are in the range of ⇩$V_{Port\_PSE\text{-}2P}$ from t_0 to the conclusion of the test.

PSE Type	Type 3	Type 4
⇩$V_{Port\_PSE\text{-}2P}$ (V)	50 – 57	52 – 57

10 PSE DLL Test suite

The following tests are based on the requirements in IEEE Std 802.3bt™-2018 Clause 145.5 and Clause 79.

10.1 PSE DLL Test 1 Send initial Power via MDI frame

This test checks whether the PSE sends out an initial Power via MDI frame within 10 seconds of the link coming up.

Last modification: Initial version.

History of changes: —

Test applicable to: PSEs that indicate DLL capability.

Test setup: Connect the SSPD model to the PSE.

Test procedure:

1. Enable to PSE and wait for the PD test fixture to be powered up.
2. Wait until at least one Power via MDI LLDP frame is received.
3. Disconnect the SSDP model.
4. Wait at least 1 s.
5. Connect the SSPD model to the PSE and wait for the model to be powered up.
6. Wait for the Ethernet link to be established.
7. Receive Power via MDI LLDP frames until either:
   - a frame is received
   - 30 seconds have passed

   Label this frame1. Mark as t_0 the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.

Pass requirements:

- All received Power via MDI frames meet the requirements in Section 8.3.1.
- $t_0 < 10\,s$

10.2 PSE DLL Test 2 PSE DLL Power Update

This test checks for the PSE to send an LLDPDU containing a Power via MDI TLV with an updated value for the 'PSE allocated power value' field within 10 seconds of receiving an LLDPDU containing a Power via MDI TLV where the 'PD requested power value' field is different from the previously communicated value.

Last modification: Initial version.

History of changes: —

10.2.1 Test 1 — LLDP transmitted within 10s SSPD

Test applicable to: PSEs that indicate DLL capability.

Test setup: Connect the SSPD model to the PSE.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up and an Ethernet link to be established.
2. Receive Power via MDI LLDP frames until either:
   - a frame with initialized power values is received
   - 30 seconds have passed

   Label this frame1. Mark as t_0 the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.
3. Send a Power via MDI LLDP frame with the PD requested power value field set in the range of 1 through 'frame1.PD requested power value' − 1. Label this frame2.
4. Receive Power via MDI LLDP frames until either:
   - a frame is received where the PD requested power value field equals the 'frame2.PD requested power value' field
   - 30 seconds have passed

   Label this frame3. Mark as t_1 the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.

Pass requirements:

- All received Power via MDI frames meet the requirements in Section 8.3.1
- 'frame3.PD requested power value' equals 'frame2.PD requested power value'
- $t_0 < 10\,s$
- $t_1 < 10\,s$

10.2.2 Test 2 — DLL Power decrease SSPD

Test applicable to: PSEs that indicate DLL capability.

Test setup: Connect the SSPD model to the PSE.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up and an Ethernet link to be established.
2. Receive Power via MDI LLDP frames until either:
   - a frame with initialized power values is received
   - 30 seconds have passed

   Label this frame1. Mark as t_0 the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.
3. Send a Power via MDI LLDP frame with the PD requested power value field set in the range of 1 through 'frame1.PD requested power value' − 1. Label this frame2.
4. Receive Power via MDI LLDP frames until either:
   - a frame is received where the PD requested power value field equals 'frame2.PD requested power value'
   - 30 seconds have passed

   Label this frame3. Mark as t_1 the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.

Pass requirements:

- All received Power via MDI frames meet the requirements in Section 8.3.1.
- 'frame3.PD requested power value' equals 'frame2.PD requested power value'
- $t_0 < 10\,s$
- $t_1 < 10\,s$

10.2.3 Test 3 — DLL Power increase SSPD

Test applicable to: PSEs that indicate DLL capability.

Test setup: Connect the SSPD model to the PSE.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up and an Ethernet link to be established.
2. Receive Power via MDI LLDP frames until either:
   - a frame with initialized power values is received
   - 30 seconds have passed

   Label this frame1. Mark as t_0 the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.
3. Send a Power via MDI LLDP frame with the PD requested power value field set to less than'frame1.PD requested power value'. Label this frame2.
4. Receive Power via MDI LLDP frames until either:
   - a frame is received where the PSE allocated power value equals 'frame2.PD requested power value'
   - 30 seconds have passed

   Label this frame3. Mark as t_1 the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.
5. Send a Power via MDI LLDP frame with the PD requested power value field set to a value higher than 'frame2.PD requested power value' but less or equal to 'frame1.PD requested power value'. Label this frame4.
6. Receive Power via MDI LLDP frames until either:
   - a Power via MDI LLDP frame is received where the PD requested power value field equals 'frame4.PD requested power value'
   - 30 seconds have passed

   Label this frame5. Mark as t_2 the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.

Pass requirements:

- All received Power via MDI frames meet the requirements in Section 8.3.1
- 'frame5.PD requested power value' equals 'frame4.PD requested power value'
- $t_0 < 10\,s$
- $t_1 < 10\,s$
- $t_2 < 10\,s$

10.2.4 Test 4 — LLDP transmitted within 10s DSPD

Test applicable to: PSEs that indicate DLL capability and PSE Logo Class 5 or greater.

Test setup: Connect the DSPD model to the PSE.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up and an Ethernet link to be established.
2. Receive Power via MDI LLDP frames until either:
   - a frame with initialized power values is received
   - 30 seconds have passed

   Label this frame1.
3. Send a Power via MDI LLDP frame where
   - PD requested power value Mode A differs from 'frame1.PD requested power value Mode A'
   - PD requested power value Mode B differs from 'frame1.PD requested power value Mode B'

   and mark this time as t_0. Label this frame2.
4. Receive Power via MDI LLDP frames until either:
   - a frame is received where both
     - PD requested power value Mode A equals frame2.PD requested power value Mode A
     - PD requested power value Mode B equals frame2.PD requested power value Mode B
   - 30 seconds have passed

   Mark this time as t_1. Label this frame3.

Pass requirements:

- All received Power via MDI frames meet the requirements in Section 8.3.1
- 'frame3.PD requested power value Mode A and Mode B' equals 'frame2.PD requested power value Mode A and Mode B'
- $t_1 - t_0 < 10\,s$

10.2.5 Test 5 — DLL Power decrease DSPD

Test applicable to: PSEs that indicate DLL capability and PSE Logo Class 5 or greater.

Test setup: Connect the DSPD model to the PSE.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up and an Ethernet link to be established.
2. Receive Power via MDI LLDP frames until either:
   - a frame with initialized power values is received
   - 30 seconds have passed

   Label this frame1.
3. Send a Power via MDI LLDP frame with PD requested power value Mode A field set less than 'frame1.PD requested power value Mode A'. Label this frame2.
4. Receive Power via MDI LLDP frames until either:
   - a frame is received with PD requested power value Mode A field equal to 'frame2.PD requested power value Mode A'
   - 30 seconds have passed

   Label this frame3. Mark as t_0 the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.
5. Send a Power via MDI LLDP frame with PD requested power value Mode B field set less than 'frame1.PD requested power value Mode B'. Label this frame4.
6. Receive Power via MDI LLDP frames until either:
   - a frame is received where the PD requested power value Mode B field equals 'frame4.PD requested power value Mode B'
   - 30 seconds have passed

   Label this frame5. Mark as t_1 the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.

Pass requirements:

- All received Power via MDI frames meet the requirements in Section 8.3.1
- 'frame3.PD requested power value Mode A' equals 'frame2.PD requested power value Mode A'
- 'frame5.PD requested power value Mode B' equals 'frame4.PD requested power value Mode B'
- $t_0 < 10\,s$
- $t_1 < 10\,s$

10.2.6 Test 6 — DLL Power increase DSPD

Test applicable to: PSEs that indicate DLL capability and PSE Logo Class 5 or greater.

Test setup: Connect the DSPD model to the PSE.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up and an Ethernet link to be established.
2. Receive Power via MDI LLDP frames until either:
   - a frame with initialized power values is received
   - 30 seconds have passed

   Label this frame1.
3. Send a Power via MDI LLDP frame with the PD requested power value Mode A field less than 'frame1.-PD requested power value Mode A'. Label this frame2.
4. Receive Power via MDI LLDP frames until either:
   - a frame with PD requested power value Mode A field equal to 'frame2.PD requested power value Mode A' is received
   - 30 seconds have passed

   Label this frame3. Mark as t_0 the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.
5. Send a Power via MDI LLDP frame with the PD requested power value Mode B field less 'frame1.PD requested power value Mode B'. Label this frame4.
6. Receive Power via MDI LLDP frames until either:
   - a frame with PD requested power value Mode B field equal to 'frame4.PD requested power value Mode B' is received
   - 30 seconds have passed

   Label this frame5. Mark as t_1 the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.
7. Send a Power via MDI LLDP frame with PD requested power value Mode A field set higher than 'frame2.PD requested power value Mode A' but not greater than 'frame1.PD requested power value Mode A'. Label this frame6.
8. Receive Power via MDI LLDP frames until either:
   - a frame with the PD requested power value Mode A field equal to 'frame6.PD requested power value Mode A' is received
   - 30 seconds have passed

   Label this frame7. Mark as t_2 the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.
9. Send a Power via MDI LLDP frame with the PD requested power value Mode B field set higher than 'frame4.PD requested power value Mode B' but less than 'frame1.PD requested power value Mode B'. Label this frame8.

10. Receive Power via MDI LLDP frames until either:
    - a frame with the PD requested power value Mode B field equal to ‘frame8.PD requested power value Mode B’ is received
    - 30 seconds have passed

    Label this frame9. Mark as t_3 the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.

Pass requirements:

- All received Power via MDI frames meet the requirements in Section 8.3.1
- ‘frame3.PD requested power value Mode A’ equals ‘frame2.PD requested power value Mode A’
- ‘frame5.PD requested power value Mode B’ equals ‘frame4.PD requested power value Mode B’
- ‘frame7.PD requested power value Mode A’ equals ‘frame6.PD requested power value Mode A’
- ‘frame9.PD requested power value Mode B’ equals ‘frame8.PD requested power value Mode B’
- $t_0 < 10\,s$
- $t_1 < 10\,s$
- $t_2 < 10\,s$
- $t_3 < 10\,s$

10.3 PSE DLL Test 3 12 Octet Power via MDI TLV

This test checks the PSE does not discard 12 octet Power Via MDI TLVs.

Last modification: Initial version.

History of changes: —

Test applicable to: PSEs that indicate DLL capability.

Test setup: Connect the SSPD model to the PSE with pd_req_class set to 4.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up and an Ethernet link to be established.
2. Receive Power via MDI LLDP frames until either:
   - a Power via MDI LLDP frame with initialized power values is received
   - 30 seconds have passed

   Label this frame1.
3. Send a Power via MDI TLV where
   - The information string length field is set to 12
   - Only the fields up until (and including) PSE allocated power value are included
   - PD requested power value is set in the range of 1 through 130

   Label this as frame 2.
4. Receive Power via MDI LLDP frames until either:
   - a Power via MDI TLV where the PD requested power value field equals ‘frame2.PD requested power value’ is received
   - 30 seconds have passed

   Label this frame3. Mark as t_0 the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.

Pass requirements:

- All received Power via MDI frames meet the requirements in Section 8.3.1.
- All PSE transmitted TLV information string length equals 29 octets or 12 octets.
- ‘frame3.PD requested power value’ = ‘frame2.PD requested power value’
- $t_0 < 10\,s$

10.4 PSE DLL Test 4 Autoclass

These tests check the PSE's handling of DLL Autoclass.

Last modification: Initial version.

History of changes: —

Test applicable to: PSEs that indicate DLL capability.

10.4.1 Test 1 — Non Physical Layer Autoclass PDs

Test setup: Connect the SSPD model to the PSE with pd_req_class set to the PSE Logo Class.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up and an Ethernet link to be established.
2. Receive Power via MDI LLDP frames until either:
   - a frame with initialized power values is received
   - 30 seconds have passed

   Label this frame1.
3. If 'frame1.PSE Autoclass support' is set to 0 the test is concluded (pass requirements do not apply), otherwise continue.
4. Send a Power via MDI LLDP frame with the following fields set:
   - PD requested power value = 0xACAC
   - Autoclass request is set

   Label this frame2.
5. Receive Power via MDI LLDP frames until either:
   - a frame is received where Autoclass completed is set
   - 30 seconds have passed

   Label this frame3. Mark as t_0 the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.
6. Send a Power via MDI LLDP frame with the following fields set:
   - PD requested power value = 0xACAC
   - Autoclass request is not set

   Label this frame4.
7. Receive Power via MDI LLDP frames until either:
   - a Power via MDI LLDP frame is received where Autoclass completed is not set
   - 30 seconds have passed

   Label this frame5. Mark as t_1 the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.

Pass requirements:

- All received Power via MDI frames meet the requirements of Section 8.3.1
- 'frame1.PSE Autoclass support' bit is set
- 'frame1.Autoclass completed' bit is not set
- 'frame1.PSE allocated power value' and 'frame1.PD requested power value' match with the assigned Class per Table 21 and Table 24
- Frame3 was received in step 5 with the Autoclass completed bit set
- Frame5 was received in step 7 with the Autoclass completed bit not set
- 'frame3.PSE allocated power value' equals 0xACAC
- 'frame5.PSE allocated power value' equals 0xACAC
- 'frame3.PD requested power value' equals 0xACAC
- 'frame5.PD requested power value' equals 0xACAC
- $t_0 < 10\,s$
- $t_1 < 10\,s$

10.4.2 Test 2 — Physical Layer Autoclass PDs

Test setup: Connect the SSPD model to the PSE with pd_req_class set to the PSE Logo Class and sspd_autoclass set to TRUE.

Test procedure:

1. Enable the PSE and wait for the PD test fixture to be powered up and an Ethernet link to be established.
2. Receive Power via MDI LLDP frames until either:
   - a frame with initialized power values
   - 30 seconds have passed

   Label this frame1.
3. If 'frame1.PSE Autoclass support' is set to 0 the test is concluded (pass requirements do not apply), otherwise continue.
4. Send a Power via MDI LLDP frame with the following fields set:
   - PD requested power value = 0xACAC
   - Autoclass request is set

   Label this frame2.
5. Receive Power via MDI LLDP frames until either:
   - a frame is received where Autoclass completed is set is received
   - 30 seconds have passed

   Label this frame3. Mark as t_0 the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.
6. Send a Power via MDI LLDP frame with the following fields set:

- PD requested power value = 0xACAC
- Autoclass request is not set

Label this frame4.

7. Receive Power via MDI LLDP frames until either:
   - a frame is received where Autoclass completed is not set is received
   - 30 seconds have passed

   Label this frame5. Mark as t_1 the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.

Pass requirements:

- All received Power via MDI frames meet the requirements of Section 8.3.1
- 'frame1.PSE Autoclass support' bit is set
- 'frame1.Autoclass completed' bit is not set
- 'frame1.PSE allocated power value' and 'frame1.PD requested power value' are set to 0xACAC
- Frame3 was received in step 5 with the Autoclass completed bit set
- Frame5 was received in step 7 with the Autoclass completed bit not set
- 'frame3.PSE allocated power value' equals 0xACAC
- 'frame5.PSE allocated power value' equals 0xACAC
- 'frame3.PD requested power value' equals 0xACAC
- 'frame5.PD requested power value' equals 0xACAC
- $t_0 < 10\,s$
- $t_1 < 10\,s$

11 Single-signature PD Test suite

The following tests compose the test plan for single-signature PDs.

11.1 PD1 Accept power

This test is for PICS PD1, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.2.

Requirement from IEEE Std 802.3bt™-2018
PDs shall be capable of accepting power in any valid 2-pair configuration and any valid 4-pair configuration as defined in Table 145–20.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.2 PD2 Two positive pairs

This test is for PICS PD2, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.2.

Requirement from IEEE Std 802.3bt™-2018

A PD shall meet the requirements of detection (145.3.4), PD signature configuration (145.3.5), and PD classification (145.3.6) in any valid 2-pair configuration, as defined in Table 145–20.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.3 PD3 Meet specification related to current (single-signature PD)

This test is for PICS PD3, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.2.

Requirement from IEEE Std 802.3bt™-2018

A single-signature PD shall meet all specifications related to current by meeting the specified total current, where total current is the combined current of the two pairs at the same polarity, unless otherwise noted (see 145.3.8.9).

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.4 PD4 Meet specification related to current (dual-signature PD)

This test is for PICS PD4, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.2.

Requirement from IEEE Std 802.3bt™-2018
A dual-signature PD shall meet all specifications related to current by meeting the specified current on the negative pair of a given Mode, unless otherwise noted (see 145.3.8.9).

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.5 PD5 Mode polarity

This test is for PICS PD5, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.2.

Requirement from IEEE Std 802.3bt™-2018
The PD shall be insensitive to the polarity of the voltage applied on each Mode regardless of the polarity of the voltage applied on the other Mode.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.6 PD6 Operation of single-signature PDs that request Class 4 or less

This test is for PICS PD6, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.2.

Requirement from IEEE Std 802.3bt™-2018
Single-signature PDs that request Class 4 or less shall be able to operate if power is supplied with any valid configuration defined in Table 145–20.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.7 PD7 Source power

This test is for PICS PD7, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.2.

Requirement from IEEE Std 802.3bt™-2018
The PD shall not source power on its PI.

Last modification: Initial version.

History of changes: —

Test applicable to: All PDs.

Test setup: Connect the PSE model to the PD with the following modifications:

- Set $R_{PSEpair1}$, $R_{PSEpair2}$, $R_{PSEpair3}$ and $R_{PSEpair4}$ to 0 Ω.
- Set S_{pair1}, S_{pair2}, S_{pair3}, and S_{pair4} to position “X”.
- Set R_{ModeA} and R_{ModeB} to 100 kΩ.
- If the PD has an alternate non-PoE power source, use it to power the PD.

Test procedure: Measure V_{PDPI_A} and V_{PDPI_B}.

Pass requirements:

- V_{PDPI_A} and V_{PDPI_B} are less than 2.8 V

11.8 PD8 Voltage tolerance

This test is for PICS PD8, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.2.

> Requirement from IEEE Std 802.3bt™-2018
>
> The PD shall withstand any voltage from 0 V to 57 V applied to the PD PI per any of the valid configurations defined in Table 145–20 indefinitely without permanent damage.

Last modification: Initial version.

History of changes: —

Test applicable to: All PDs.

Test order execution: This test is to be executed before others.

Test setup: Connect the PSE model to PD in the following configuration:

- Powering configuration PD_PCFG2–1 (see Table 7)
- S_{altA} and S_{altB} set to position "R"
- $R_{PSEpair1}$, $R_{PSEpair2}$, $R_{PSEpair3}$, and $R_{PSEpair4}$ are set to 0.25 Ω or less

Test procedure:

1. Slew V_{supply} to rise from 0 V to be greater than 55 V but less than 57 V with a linear slew of 1 ms.
2. Wait at least 5 s.
3. Set V_{supply} to 0 V.
4. Slew V_{supply} to rise from 0 V to be greater than 55 V but less than 57 V with a linear slew of at least 5 s.
5. Wait at least 5 s.
6. Set V_{supply} to 0 V.
7. ↻ Repeat the test for each of the power configurations shown in Table 7.

Pass requirements: The PD passes all subsequent tests. No specific requirements from this test.

11.9 PD9 Single-signature PD behavior

This test is for PICS PD9, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.3.3.

Requirement from IEEE Std 802.3bt™-2018
Single-signature PDs shall provide the behavior of the state diagram shown in Figure 145–25 and Figure 145–26.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.10 PD10 Dual-signature PD behavior

This test is for PICS PD10, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.3.4.

Requirement from IEEE Std 802.3bt™-2018

Dual-signature PDs shall provide the behavior of the state diagram shown in Figure 145–27 over each pairset independently unless otherwise specified.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.11 PD11 Valid and non-valid detection signatures

This test is for PICS PD11, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.4.

Requirement from IEEE Std 802.3bt™-2018

When a PD presents a valid or non-valid detection signature, it shall present the detection signature at the PI between Positive V_{PD} and Negative V_{PD} of PD Mode A and PD Mode B as defined in 145.3.2.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.12 PD12 Valid detection signature powering conditions

This test is for PICS PD12, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.4.

Requirement from IEEE Std 802.3bt™-2018

While a PD presents a valid detection signature on a given Mode, that detection signature shall be valid when presented under each of the following conditions (see Figure 145–28):

- with any resistance greater than 45 kΩ across the other Mode
- with any resistance greater than 45 kΩ across the other Mode and one pair connected to the positive potential of the given Mode

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

11.12.1 Test 1 — Input capacitance

Test setup:

- Connect a capacitance meter between pair1 and pair2 of the PD
- Capacitance measurements must occur with a voltage in the range of 2.7 V to 10.1 V applied across the pairs

Test procedure:

1. Measure the capacitance between pair1 and pair2 and record as $C_{detect1}$.
2. Disconnect the capacitance meter and connect between pair3 and pair 4.
3. Measure the capacitance between pair3 and pair4 and record as $C_{detect2}$.

Pass requirements: $C_{detect1}$ and $C_{detect2}$ are in the range of 50 nF to 120 nF

11.12.2 Test 2 — Mode A

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG2–1
- R_{ModeB} is set to 45 kΩ to 46 kΩ

Test procedure:

1. Set S_{altA} to the 'V' position.
2. Set V_{altA} such that V_{PSE_A} is 2.91 V ± 100 mV.
3. Measure $I_{pair\_negative\_A}$ and record as $I_{detect1}$.
4. Measure V_{PDPI_A} and record as $V_{detect1}$.

5. Set V_{altA} such that V_{PSE_A} is 4.11 V ± 100 mV.
6. Measure $I_{pair\_negative\_A}$ and record as $I_{detect2}$.
7. Measure V_{PDPI_A} and record as $V_{detect2}$.
8. Let $R_{detect1} = |(V_{detect2} - V_{detect1})/(I_{detect2} - I_{detect1})|$.
9. Set V_{altA} such that V_{PSE_A} is 8.8 V ± 100 mV.
10. Measure $I_{pair\_negative\_A}$ and record as $I_{detect3}$.
11. Measure V_{PDPI_A} and record as $V_{detect3}$.
12. Adjust V_{altA} such that V_{PSE_A} is 10 V ± 100 mV.
13. Measure $I_{pair\_negative\_A}$ and record as $I_{detect4}$.
14. Measure V_{PDPI_A} and record as $V_{detect4}$.
15. Let $R_{detect2} = |(V_{detect4} - V_{detect3})/(I_{detect4} - I_{detect3})|$.
16. Let $R_{detect3} = |(V_{detect4} - V_{detect1})/(I_{detect4} - I_{detect1})|$.
17. Let $V_{offset1} = |V_{detect4}| - (|I_{detect4}| \times R_{detect3})$.
18. Adjust V_{altA} such that $I_{pair\_negative\_A} = 134\ \mu A \pm 10\ \mu A$.
19. Measure V_{PDPI_A} and record as V_{PI}.
20. Set V_{altA} such that V_{PSE_A} is 0 V.
21. ↻ Repeat steps 2 to 20 for each power configuration listed in Table 37.

Pass requirements:

- Each of the calculated resistances $R_{detect1}$, $R_{detect2}$, and $R_{detect3}$ are in the range of 23.7 kΩ to 26.3 kΩ [⇨R_{detect}]
- Each of the calculated voltages $V_{offset1}$ are in the range of 0 V to 1.9 V [⇨V_{offset}]
- V_{PI} is greater than 2.7 V

11.12.3 Test 3 — Mode B

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG2–1
- R_{ModeA} is set to 45 kΩ to 46 kΩ

Test procedure:

1. Set S_{altB} to the 'V' position.
2. Set V_{altB} such that V_{PSE_B} is 2.91 V ± 100 mV.
3. Measure $I_{pair\_negative\_B}$ and record as $I_{detect1}$.
4. Measure V_{PDPI_B} and record as $V_{detect1}$.
5. Set V_{altB} such that V_{PSE_B} is 4.11 V ± 100 mV.

6. Measure $I_{pair\_negative\_B}$ and record as $I_{detect2}$.
7. Measure V_{PDPI_B} and record as $V_{detect2}$.
8. Let $R_{detect1} = |(V_{detect2} - V_{detect1})/(I_{detect2} - I_{detect1})|$.
9. Set V_{altB} such that V_{PSE_B} is 8.8 V ± 100 mV.
10. Measure $I_{pair\_negative\_B}$ and record as $I_{detect3}$.
11. Measure V_{PDPI_B} and record as $V_{detect3}$.
12. Adjust V_{altB} such that V_{PSE_B} is 10 V ± 100 mV.
13. Measure $I_{pair\_negative\_B}$ and record as $I_{detect4}$.
14. Measure V_{PDPI_B} and record as $V_{detect4}$.
15. Let $R_{detect2} = |(V_{detect4} - V_{detect3})/(I_{detect4} - I_{detect3})|$.
16. Let $R_{detect3} = |(V_{detect4} - V_{detect1})/(I_{detect4} - I_{detect1})|$.
17. Let $V_{offset1} = |V_{detect4}| - (|I_{detect4}| \times R_{detect3})$.
18. Adjust V_{altB} such that $I_{pair\_negative\_B} = 134\ \mu A \pm 10\ \mu A$.
19. Measure V_{PDPI_B} and record as V_{PI}.
20. Set V_{altB} such that V_{PSE_B} is 0 V.
21. ↻ Repeat steps 2 to 20 for each power configuration listed in Table 38.

Pass requirements:

- Each of the calculated resistances $R_{detect1}$, $R_{detect2}$, and $R_{detect3}$ are in the range of 23.7 kΩ to 26.3 kΩ [⇨R_{detect}]
- Each of the calculated voltages $V_{offset1}$ are in the range of 0 V to 1.9 V [⇨V_{offset}]
- V_{PI} is greater than 2.7 V

Table 37: PD12 Mode A detection

Power Configuration
PD_PCFG2-1
PD_PCFG2-2
PD_PCFG3–1
PD_PCFG3–2
PD_PCFG3–3
PD_PCFG3–4

Table 38: PD12 Mode B detection

Power Configuration
PD_PCFG2-3
PD_PCFG2-4
PD_PCFG3–5
PD_PCFG3–6
PD_PCFG3–7
PD_PCFG3–8

11.13 PD13 Single-signature PDs powered over only one pairset

This test is for PICS PD13, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.4.

> Requirement from IEEE Std 802.3bt™-2018
>
> A single-signature PD that is powered over only one pairset shall present a non-valid detection signature on the unpowered pairset.

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

Test setup: Connect the PSE model to the PD using power configuration PD_PCFG4–1 (see Table 7).

11.13.1 Test 1 — Detection on Mode A

Test procedure:

1. Apply a classification, inrush, and power on waveform as described in Section 7 on Mode B.
2. After power on, adjust V_{supply} such that V_{PSE_B} is in the range of 52 V to 57 V.
3. Measure the capacitance between nodes pair1 and pair2 and record as $C_{detect1}$.
4. Set S_{altA} to 'V' position.
5. Set V_{altA} such that V_{PSE_A} is 2.91 V ± 100 mV.
6. Measure $I_{pair\_negative\_A}$ and record as $I_{detect1}$.
7. Measure V_{PDPI_A} and record as $V_{detect1}$.
8. Set V_{altA} such that V_{PSE_A} is 4.11 V ± 100 mV.
9. Measure $I_{pair\_negative\_A}$ and record as $I_{detect2}$.
10. Measure V_{PDPI_A} and record as $V_{detect2}$.
11. Let $R_{detect1} = |(V_{detect2} - V_{detect1})/(I_{detect2} - I_{detect1})|$.
12. Set V_{altA} such that V_{PSE_A} is 8.8 V ± 100 mV.
13. Measure $I_{pair\_negative\_A}$ and record as $I_{detect3}$.
14. Measure V_{PDPI_A} and record as $V_{detect3}$.
15. Set V_{altA} such that V_{PSE_A} is 10 V ± 100 mV.
16. Measure $I_{pair\_negative\_A}$ and record as $I_{detect4}$.
17. Measure V_{PDPI_A} and record as $V_{detect4}$.
18. Let $R_{detect2} = |(V_{detect4} - V_{detect3})/(I_{detect4} - I_{detect3})|$.
19. Let $R_{detect3} = |(V_{detect4} - V_{detect1})/(I_{detect4} - I_{detect1})|$.
20. ↻ Repeat this test using power configuration PD_PCFG4–2, PD_PCFG4–3, and PD_PCFG4–4 (see Table 7).

Pass requirements: Either or both of the following holds:

- $C_{detect1} > 10\,\mu F$
- $R_{detect1}$, $R_{detect2}$, and $R_{detect3}$ are not in the range of 12 kΩ to 45 kΩ

11.13.2 Test 2 — Detection on Mode B

Test procedure:

1. Apply a classification, inrush, and power on waveform as described in Section 7 on Mode A.
2. After power on, adjust V_{supply} such that V_{PSE_A} is in the range of 52 V to 57 V.
3. Measure the capacitance between nodes pair3 and pair4 and record as $C_{detect1}$.
4. Set S_{altB} to the 'V' position.
5. Set V_{altB} such that V_{PSE_B} is 2.91 V ± 100 mV.
6. Measure $I_{pair\_negative\_B}$ and record as $I_{detect1}$.
7. Measure V_{PDPI_B} and record as $V_{detect1}$.
8. Set V_{altB} such that V_{PSE_B} is 4.11 V ± 100 mV.
9. Measure $I_{pair\_negative\_B}$ and record as $I_{detect2}$.
10. Measure V_{PDPI_B} and record as $V_{detect2}$.
11. Let $R_{detect1} = |(V_{detect2} - V_{detect1})/(I_{detect2} - I_{detect1})|$.
12. Set V_{altB} such that V_{PSE_B} is 8.8 V ± 100 mV.
13. Measure $I_{pair\_negative\_B}$ and record as $I_{detect3}$.
14. Measure V_{PDPI_B} and record as $V_{detect3}$.
15. Set V_{altB} such that V_{PSE_B} is 10 V ± 100 mV.
16. Measure $I_{pair\_negative\_B}$ and record as $I_{detect4}$.
17. Measure V_{PDPI_B} and record as $V_{detect4}$.
18. Let $R_{detect2} = |(V_{detect4} - V_{detect3})/(I_{detect4} - I_{detect3})|$.
19. Let $R_{detect3} = |(V_{detect4} - V_{detect1})/(I_{detect4} - I_{detect1})|$.
20. ↻ Repeat this test using power configuration PD_PCFG4–2, PD_PCFG4–3, and PD_PCFG4–4 (see Table 7).

Pass requirements: Either or both of the following holds:

- $C_{detect1} > 10\,\mu F$
- $R_{detect1}$, $R_{detect2}$, and $R_{detect3}$ are not in the range of 12 kΩ to 45 kΩ

11.14 PD14 Dual-signature PDs powered over only one pairset

This test is for PICS PD14, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.4.

Requirement from IEEE Std 802.3bt™-2018
A dual-signature PD that is powered over only one pairset shall present a valid detection signature on the unpowered pairset.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.15 PD15 Valid detection signature

This test is for PICS PD15, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.4.

Requirement from IEEE Std 802.3bt™-2018
A valid PD detection signature shall have the characteristics of Table 145–21.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.16 PD16 Non-valid detection signature

This test is for PICS PD16, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.4.

Requirement from IEEE Std 802.3bt™-2018
A non-valid detection signature shall have one or both of the characteristics in Table 145–22.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.17 PD17 Single-signature PD configuration

This test is for PICS PD17, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.5.

Requirement from IEEE Std 802.3bt™-2018

A single-signature PD shall present a valid detection signature, as defined in Table 145–21, on a given Mode when no voltage or current is applied to the other Mode...

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.18 PD18 Single-signature PD configuration

This test is for PICS PD18, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.5.

> Requirement from IEEE Std 802.3bt™-2018
>
> . . . and shall not present a valid detection signature on the given Mode when any voltage in the range of 3.7 V to 57 V is applied to the other Mode or any current greater than 124 µA is applied to the other Mode.

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

Test setup: Connect the PSE model to the PD using power configuration PD_PCFG4–1 (see Table 7).

11.18.1 Test 1 — Mode A

Test procedure:

1. Set V_{altB} such that $|V_{PDPI\_B}|$ is 3.8 V ± 100 mV.
2. Set V_{altA} such that V_{PSE_A} is 2.91 V ± 100 mV.
3. Measure $I_{pair\_negative\_A}$ and record as $I_{detect1}$.
4. Measure V_{PDPI_A} and record as $V_{detect1}$.
5. Set V_{altA} such that V_{PSE_A} is 4.11 V ± 100 mV.
6. Measure $I_{pair\_negative\_A}$ and record as $I_{detect2}$.
7. Measure V_{PDPI_A} and record as $V_{detect2}$.
8. Let $R_{detect1} = |(V_{detect2} - V_{detect1})/(I_{detect2} - I_{detect1})|$.
9. Set V_{altA} such that V_{PSE_A} is 8.8 V ± 100 mV.
10. Measure $I_{pair\_negative\_A}$ and record as $I_{detect3}$.
11. Measure V_{PDPI_A} and record as $V_{detect3}$.
12. Set V_{altA} such that V_{PSE_A} is 10 V ± 100 mV.
13. Measure $I_{pair\_negative\_A}$ and record as $I_{detect4}$.
14. Measure V_{PDPI_A} and record as $V_{detect4}$.
15. Let $R_{detect2} = |(V_{detect4} - V_{detect3})/(I_{detect4} - I_{detect3})|$.
16. Let $R_{detect3} = |(V_{detect4} - V_{detect1})/(I_{detect4} - I_{detect1})|$.
17. Let $V_{offset1} = |V_{detect4}| - |I_{detect4}| \times R_{detect3}$.
18. Set V_{altA} such that $|I_{pair\_negative\_A}| = 134\ \mu A \pm 10\ \mu A$.
19. Measure V_{PDPI_A} and record as V_{PI}.
20. ↻ Repeat this test using power configuration PD_PCFG4–2, PD_PCFG4–3, and PD_PCFG4–4 (see Table 7).

Pass requirements: At least one of the following must hold:

- $R_{detect1}$, $R_{detect2}$, and $R_{detect3}$ are not in the range of 23.7 kΩ to 26.3 kΩ
- $V_{offset1}$ is greater than 1.9 V [⇨V_{offset} max]
- V_{PI} is less than 2.7 V

11.18.2 Test 2 — Mode B

Test procedure:

1. Set V_{altA} such that V_{PSE_A} is 3.8 V ± 100 mV.
2. Set V_{altB} such that V_{PSE_B} is 2.91 V ± 100 mV.
3. Measure $I_{pair\_negative\_B}$ and record as $I_{detect1}$.
4. Measure V_{PDPI_B} and record as $V_{detect1}$.
5. Set V_{altB} such that V_{PSE_B} is 4.11 V ± 100 mV.
6. Measure $I_{pair\_negative\_B}$ and record as $I_{detect2}$.
7. Measure V_{PDPI_B} and record as $V_{detect2}$.
8. Let $R_{detect1} = |(V_{detect2} - V_{detect1})/(I_{detect2} - I_{detect1})|$.
9. Set V_{altB} such that V_{PSE_B} is 8.8 V ± 100 mV.
10. Measure $I_{pair\_negative\_B}$ and record as $I_{detect3}$.
11. Measure V_{PDPI_B} and record as $V_{detect3}$.
12. Set V_{altB} such that V_{PSE_B} is 10 V ± 100 mV.
13. Measure $I_{pair\_negative\_B}$ and record as $I_{detect4}$.
14. Measure V_{PDPI_B} and record as $V_{detect4}$.
15. Let $R_{detect2} = |(V_{detect4} - V_{detect3})/(I_{detect4} - I_{detect3})|$.
16. Let $R_{detect3} = |(V_{detect4} - V_{detect1})/(I_{detect4} - I_{detect1})|$.
17. Let $V_{offset1} = |V_{detect4}| - |I_{detect4}| \times R_{detect3}$.
18. Adjust V_{altB} such that $|I_{pair\_negative\_B}|$ is 134 µA ± 10 µA.
19. Measure V_{PDPI_B} and record as V_{PI}.
20. ↻ Repeat this test using power configuration PD_PCFG4–2, PD_PCFG4–3, and PD_PCFG4–4 (see Table 7).

Pass requirements: At least one of the following must hold:

- $R_{detect1}$, $R_{detect2}$, and $R_{detect3}$ are not in the range of 23.7 kΩ to 26.3 kΩ
- $V_{offset1}$ is greater than 1.9 V [⇨V_{offset} max]
- V_{PI} is less than 2.7 V

11.19 PD19 Dual-signature PD configuration

This test is for PICS PD19, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.5.

Requirement from IEEE Std 802.3bt™-2018

A dual-signature PD shall present a valid detection signature, as defined in Table 145–21, on a given Mode, regardless of any voltage between 0 V and 57 V applied to the other Mode.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.20 PD20 Maximum power drawn

This test is for PICS PD20, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.6.

Requirement from IEEE Std 802.3bt™-2018

The PD shall draw no more power across any voltage in the range of $V_{Port\_PD\text{-}2P}$ than defined for the requested Class in Table 145–26 and Table 145–27.

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG4–2 (see Table 7)
- V_{supply} set to a voltage in the range of $\Rightarrow V_{Port\_PSE\text{-}2P}$ min to $\Rightarrow V_{Port\_PSE\text{-}2P}$ min + 200 mV
- $R_{PSEpair1}$, $R_{PSEpair2}$, $R_{PSEpair3}$, and $R_{PSEpair4}$ set in the range of 5 Ω to 6.25 Ω
- class_event_count set to 6

Requested Class	1 to 6	7 to 8
$\Rightarrow V_{Port\_PSE\text{-}2P}$ min (V)	50	52

Test procedure:

1. Apply a classification, inrush, and power on waveform.
2. Determine pd_req_class.
3. Wait for at least 10 s.
4. Measure the highest average power (see 6.1.6) and record this as p_0.
5. Power down the PD and wait for at least the inter-test wait time specified in Section 4.4.

Pass requirements: The highest average PD power p_0 is below [$\Rightarrow P_{Class\_PD}$] for pd_req_class.

Requested Class	1	2	3	4	5	6	7	8
$\Rightarrow P_{Class\_PD}$ (W)	3.84	6.49	13	25.5	40	51	62	71.3

11.21 PD21 Conform to the assigned Class

This test is for PICS PD21, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.6.

Requirement from IEEE Std 802.3bt™-2018
The PD shall conform to the assigned Class, regardless of its requested Class.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.22 PD22 Multiple-Event classification

This test is for PICS PD22, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.6.

Requirement from IEEE Std 802.3bt™-2018
PDs shall provide Multiple-Event Physical Layer classification as defined in 145.3.6.1.

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

Test applicable to: No test is required.

11.23 PD23 Data Link Layer classification

This test is for PICS PD23, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.6.

Requirement from IEEE Std 802.3bt™-2018
Single-signature PDs that request Class 4 or higher and dual-signature PDs that request Class 4 or higher on at least one of its Modes shall provide DLL classification.

Last modification: Initial version.

History of changes: —

Test applicable to: Single-signature PDs with PD Logo Class 4 or higher

Test applicable to: No test is required.

11.24 PD24 PD classification behavior

This test is for PICS PD24, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.6.

Requirement from IEEE Std 802.3bt™-2018
PD classification behavior shall conform to the state diagram in Figure 145–25 or Figure 145–27,...

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

Test applicable to: No test is required.

11.25 PD25 PD classification electrical specifications

This test is for PICS PD25, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.6.

Requirement from IEEE Std 802.3bt™-2018
. . . and shall conform to the electrical specifications defined in Table 145–24 and Table 145–25.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.26 PD26 Underpowered PDs

This test is for PICS PD26, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.6.

Requirement from IEEE Std 802.3bt™-2018
A PD that is assigned to a Class lower than the Class it requested shall provide the user with an active indication if underpowered.

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

Test applicable to: No test is required.

11.27 PD27 Class signature presented during classification events

This test is for PICS PD27, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.6.1.

> Requirement from IEEE Std 802.3bt™-2018
>
> PDs shall present class_sig_A during DO_CLASS_EVENT1 and DO_CLASS_EVENT2 and class_sig_B during DO_CLASS_EVENT3, DO_CLASS_EVENT4, DO_CLASS_EVENT5, and DO_CLASS_EVENT6, as shown in Figure 145–25 and Figure 145–27, with the corresponding classification signatures specified in Table 145–24.

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG2–1 as listed in Table 7
- class_event_count is set to 6

Test procedure:

1. Apply a classification waveform and hold the PSE voltage in the mark range at the final mark event.
2. Set V_{altA} and/or V_{altB} such that V_{PDPI} is in the range of $2.7\,V \pm 100\,mV$.
3. Wait at least 15 ms.
4. Apply a another classification waveform.
5. Set V_{altA} and/or V_{altB} such that V_{PDPI} is in the range of $2.7\,V \pm 100\,mV$.
6. Wait at least 15 ms.
7. ↻ Repeat for power configurations PD_PCFG2-4, PD_PCFG3-2, PD_PCFG3-5, and PD_PCFG4-2.

Pass requirements: For both classification waveform measurements (in step 1 and 4) it holds that:

- The six measured class currents are valid class signatures per Table 15
- The class signatures correspond with those listed in Table 39 for the PD Logo Class

Table 39: Class signature for single-signature PDs for PD27

PD Logo Class	Class signature during n^{th} class event					
	$n=1$	$n=2$	$n=3$	$n=4$	$n=5$	$n=6$
1	1	1	1	1	1	1
2	2	2	2	2	2	2
3	3	3	3	3	3	3
4	4	4	4	4	4	4
5	4	4	0	0	0	0
6	4	4	1	1	1	1
7	4	4	2	2	2	2
8	4	4	3	3	3	3

11.28 PD28 Class signature during Autoclass

This test is for PICS PD28, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.6.1.

Requirement from IEEE Std 802.3bt™-2018
PDs implementing Autoclass shall present class signature 0, as defined in Table 145–24, during DO_CLASS_EVENT_AUTO as defined in 145.3.6.2.

Last modification: Initial version.

History of changes: —

Test applicable to: Single-signature PDs that request Autoclass

Test applicable to: No test is required.

11.29 PD29 Class signature validity

This test is for PICS PD29, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.6.1.

> Requirement from IEEE Std 802.3bt™-2018
>
> After entering a DO_CLASS_EVENT state, the PD Physical Layer class signature shall be valid within T_{Class_PD} as defined in Table 145–29 and remain valid for the remainder of the class event.

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

Test setup: Connect the PSE model to the PD with the following settings:

- Any power configuration listed in Table 7
- class_event_count is set to 6
- Set T_{Class1} through T_{Class5} to 75 ms
- The class current during each class event is to measured at least 5 times, with the first measurement between 6 ms to 10 ms from the beginning of the class event, and the other measurements spread out equally over the remaining time.

Test procedure:

1. Apply a classification waveform.

Pass requirements: For each of the class events:

- all of the measured class currents represent valid class signatures (per Table 15)
- all of the resulting class signatures are the same within a single class event

11.30 PD30 Advertised class signatures for single-signature PDs

This test is for PICS PD30, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.6.1.

Requirement from IEEE Std 802.3bt™-2018
Single-signature PDs shall advertise class signatures according to the PD Type and PD requested Class, as defined in Table 145–26.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.31 PD31 Advertised class signatures for dual-signature PDs

This test is for PICS PD31, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.6.1.

Requirement from IEEE Std 802.3bt™-2018
Dual-signature PDs shall advertise class signatures according to the PD Type and PD requested Class on each pairset, as defined in Table 145–27.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.32 PD32 Dual-signature PDs powered over only one pairset

This test is for PICS PD32, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.6.1.

Requirement from IEEE Std 802.3bt™-2018
A dual-signature PD that is powered over only one pairset shall present a valid class signature on the unpowered pairset.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.33 PD33 PD current draw when in a DO_MARK_EVENT state

This test is for PICS PD33, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.6.1.1.

> Requirement from IEEE Std 802.3bt™-2018
>
> When the PD is presenting a mark event signature in a DO_MARK_EVENT state, as shown in the state diagram of Figure 145–25 and Figure 145–27, the PD shall draw I_{Mark} as defined in Table 145–25 and present a non-valid detection signature as defined in Table 145–22.

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

11.33.1 Test 1 — Mode A

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG2–1 as listed in Table 7

Test procedure:

1. Set S_{altA} to the "V" setting and V_{altA} such that V_{PDPI_A} is in the range of 14.5 V to 20.5 V [⇨V_{Class_PD}].
2. Wait for at least 10 ms.
3. Set V_{altA} such that V_{PDPI_A} is 7.5 V±100 mV.
4. Measure V_{PDPI_A} and record as $V_{detect1}$.
5. Measure $I_{pair\_negative\_A}$ and record as $I_{detect1}$.
6. Measure the capacitance between pair1 and pair2 and record as cap1.
7. Set V_{altA} such that V_{PDPI_A} is 9.5 V±100 mV.
8. Measure V_{PDPI_A} and record as $V_{detect2}$.
9. Measure $I_{pair\_negative\_A}$ and record as $I_{detect2}$.
10. Measure the capacitance between pair1 and pair2 and record as cap2.
11. Let $R_{detect1} = |(V_{detect2} - V_{detect1})/(I_{detect2} - I_{detect1})|$.
12. ↻ Repeat using power configuration PD_PCFG3–3 (see Table 7).

Pass requirements:

- $I_{detect1}$ and $I_{detect2}$ are in the range of 0.25 mA to 4 mA [⇨I_{Mark}]
- One or both of the following holds:
  - $R_{detect1}$ is not in the range of 12 kΩ to 45 kΩ
  - cap1 and cap2 are greater than 10 µF

11.33.2 Test 2 — Mode B

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG2–3 as listed in Table 7

Test procedure:

1. Set S_{altB} to the "V" setting and V_{altB} such that V_{PDPI_B} is in the range of 14.5 V to 20.5 V [⇨V_{Class_PD}].
2. Wait for at least 10 ms.
3. Set V_{altB} such that V_{PDPI_B} is 7.5 V±100 mV.
4. Measure V_{PDPI_B} and record as $V_{detect1}$.
5. Measure $I_{pair\_negative\_B}$ and record as $I_{detect1}$.
6. Measure the capacitance between pair3 and pair4 and record as cap1.
7. Set V_{altB} such that V_{PDPI_B} is 9.5 V±100 mV.
8. Measure V_{PDPI_B} and record as $V_{detect2}$.
9. Measure $I_{pair\_negative\_B}$ and record as $I_{detect2}$.
10. Measure the capacitance between pair3 and pair4 and record as cap2.
11. Let $R_{detect1} = |(V_{detect2} - V_{detect1})/(I_{detect2} - I_{detect1})|$.
12. ↻ Repeat using power configuration PD_PCFG3–6 (see Table 7).

Pass requirements:

- $I_{detect1}$ and $I_{detect2}$ are in the range of 0.25 mA to 4 mA [⇨I_{Mark}]
- One or both of the following holds:
  - $R_{detect1}$ is not in the range of 12 kΩ to 45 kΩ
  - cap1 and cap2 are greater than 10 µF

11.34 PD34 Mark event current limits

This test is for PICS PD34, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.6.1.1.

Requirement from IEEE Std 802.3bt™-2018
The PD shall not exceed the I_{Mark} current limits when voltage at the PI enters the V_{Mark_PD} specification as defined in Table 145–25.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.35 PD35 Autoclass class signature timing

This test is for PICS PD35, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.6.2.

> Requirement from IEEE Std 802.3bt™-2018
>
> A PD that implements Autoclass shall change its current during the first class event to class signature 0 no earlier than T_{ACS} min and no later than T_{ACS} max, as defined in Table 145–28.

Last modification: Initial version.

History of changes: —

Test applicable to: Single-signature PDs that request Autoclass.

Test setup: Connect the PSE model to the PD using power configuration PD_PCFG4–2 (see Table 7).

Test procedure:

1. Set V_{altA} and/or V_{altB} such that V_{PDPI_A} and/or V_{PDPI_B} are in the range of 14.5 V to 20.5 V [⇨V_{Class_PD}] and mark this time as t_0.
2. At $t_0 + 10\,ms \pm 4\,ms$ measure $I_{pair\_negative\_A}$ and $I_{pair\_negative\_B}$ and record the sum as current1.
3. At $t_0 + 74\,ms \pm 1\,ms$ measure $I_{pair\_negative\_A}$ and $I_{pair\_negative\_B}$ and record the sum as current2.
4. At $t_0 + 89\,ms \pm 1\,ms$ measure $I_{pair\_negative\_A}$ and $I_{pair\_negative\_B}$ and record the sum as current3.
5. At $t_0 + 100\,ms \pm 10\,ms$ measure $I_{pair\_negative\_A}$ and $I_{pair\_negative\_B}$ and record the sum as current4.

Pass requirements:

- current1 and current2 are not in the range of 1 mA to 4 mA [⇨PD class signature 0]
- current1 and current2 are in the same [⇨PD class signature]
- current3 and current4 are both in the range of 1 mA to 4 mA [⇨PD class signature 0]

PD class signature	0	1	2	3	4
current (mA)	1 – 4	9 – 12	17 – 20	26 – 30	36 – 44

11.36 PD36 Autoclass power draw

This test is for PICS PD36, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.6.2.

Requirement from IEEE Std 802.3bt™-2018

After power up, a PD that implements Autoclass shall draw its highest required power, $P_{Autoclass\_PD}$, subject to the requirements on P_{Class_PD} in 145.3.8.2, throughout the period bounded by T_{AUTO_PD1} and T_{AUTO_PD2}, measured from when V_{PD} rises above V_{On_PD}.

Last modification: Initial version.

History of changes: —

Test applicable to: Single-signature PDs that request Autoclass.

Test setup: Connect the PSE model to the PD using power configuration PD_PCFG4–2 (see Table 7).

Test procedure:

1. Apply a classification, inrush, and power on waveform.
2. Measure the highest average power using a window of 150 ms to 300 ms [$\Rightarrow T_{AUTO\_Window}$] from $t_{classification\_end} + 1.35\,s[\Rightarrow T_{AUTO\_PD1}]$ until $t_{classification\_end} + 3.65\,s[\Rightarrow T_{AUTO\_PD2}]$ and record this as p_0.
3. Wait at least 1 s.
4. Measure the highest average power for at least 60 s and record this as p_1.

Pass requirements: $p_1 \leq p_0$.

11.37 PD37 PSE Type identification

This test is for PICS PD37, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.7.

Requirement from IEEE Std 802.3bt™-2018

Such a PD may set long_class_event to TRUE if the first class event is longer than T_{LCE_PD} min and shall set long_class_event to TRUE if the first class event is longer than T_{LCE_PD} max.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.38 PD38 PD operation

This test is for PICS PD38, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.

Requirement from IEEE Std 802.3bt™-2018
The PD shall operate within the characteristics in Table 145–29.

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

Test applicable to: No test is required.

11.39 PD39 PD turn on voltage

This test is for PICS PD39, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.1.

Requirement from IEEE Std 802.3bt™-2018
The PD shall turn on at a voltage in the range of V_{On_PD}.

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

Test setup: Connect the PSE model to the PD using power configuration PD_PCFG4–2 (see Table 7).

Test procedure:

1. Set V_{supply} in the range of 27 V to 29 V.
2. Set S_{altA} and S_{altB} in the 'R' position.
3. Wait at least 100 ms.
4. Measure $I_{pair\_negative}$.

Pass requirements: The measured $I_{pair\_negative}$ is less than 60 mA.

11.40 PD40 PD stay on voltage

This test is for PICS PD40, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.1.

Requirement from IEEE Std 802.3bt™-2018
After the PD turns on, the PD shall stay on over the entire $V_{Port\_PD\text{-}2P}$ range.

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

Test applicable to: No test is required.

11.41 PD41 PD turn off voltage

This test is for PICS PD41, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.1.

Requirement from IEEE Std 802.3bt™-2018
After reaching POWER_DELAY, the PD shall turn off at a voltage in the range of V_{Off_PD}.

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG4–2 (see Table 7)
- V_{supply} is set in the range of 55 V to 57 V
- psemodel_max_class is set to 8

Test procedure:

1. Apply a classification, inrush, and power on waveform as described in Section 7.
2. Wait at least 10 s.
3. Reduce the V_{supply} to a voltage in the range of 29 V to 30 V [⇩V_{Off_PD} min].
4. Measure $I_{pair\_negative\_A}$ and $I_{pair\_negative\_B}$.

Pass requirements: $I_{pair\_negative} \leq 44$ mA

11.42 PD42 Peak power draw or voltage transients present

This test is for PICS PD42, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.1.

Requirement from IEEE Std 802.3bt™-2018
A PD shall not turn off due to peak power draw, causing V_{PD} to go as low as $V_{Overload-2P}$, as specified in 145.3.8.4, or due to a voltage transient as defined in 145.3.8.6.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.43 PD43 Startup oscillations

This test is for PICS PD43, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.1.

Requirement from IEEE Std 802.3bt™-2018

The PD shall turn on or off without startup oscillation and within the first trial at any load value when fed by $V_{Port\_PSE\text{-}2P}$ min to $V_{Port\_PSE\text{-}2P}$ max (as defined in Table 145–16):
– with a series resistance less than or equal to R_{Ch} for assigned Class 1 through 4 to a single-signature PD,
– with a series resistance less than or equal to R_{Ch} / 2 for assigned Class 5 through 8 to a single-signature PD,
– with a series resistance less than or equal to R_{Ch} connected to a given Mode of a dual-signature PD.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.44 PD44 P_{Port_PD} (single-signature PD)

This test is for PICS PD44, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.2.

Requirement from IEEE Std 802.3bt™-2018
For single-signature PDs, P_{Port_PD} shall not exceed P_{Class_PD} for the assigned class.

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

Test setup: Connect the PSE model to the PD.

Test procedure:

1. Set psemodel_max_class to 3.
2. Set the power configuration per the current iteration of Table 40.
   NOTE—For the first iteration this is PD_PCFG2–1.
3. Set $R_{PSEpair n}$ in the range of 0 Ω to 1 Ω.
4. Set V_{supply} between:
   - 50 V to 51 V when psemodel_max_class is less or equal to 6
   - 52 V to 53 V when psemodel_max_class is greater than 6
5. Apply a classification, inrush, and power on waveform as described in Section 7.
6. Wait at least 10 s.
7. Measure the highest average power (see 6.1.6) and record this as p_0.
8. Power down the PD and wait for at least the inter-test wait time specified in Section 4.4.
9. ↻ Repeat steps 5 through 8 for every value of psemodel_max_class listed in Table 40.
10. ↻ Repeat steps 5 through 9 with V_{supply} set to 56 V to 57 V.
11. ↻ Repeat steps 4 through 10 with $R_{PSEpair n}$ set to 5 Ω to 6.25 Ω.
12. ↻ Repeat steps 3 through 11 for the following power configurations from Table 7:
    - PD_PCFG2–1
    - PD_PCFG2–3
    - PD_PCFG3–3
    - PD_PCFG3–7
    - PD_PCFG4–1
    - PD_PCFG4–2
    - PD_PCFG4–3
    - PD_PCFG4–4

NOTE—There are 32 test permutations for PD Logo Class 3 and below, 64 test permutations for PD Logo Class 4, 80 test permutations for PD Logo Class 5 and 6, and 96 test permutations for PD Logo Class 7 and 8.

Table 40: Value permutations of psemodel_max_class per the PD Logo Class

PD Logo Class	Power configuration	Values of psemodel_max_class
1, 2, or 3	All	3
4	All	3, 4
5, 6	PD_PCFG2–*x* or PD_PCFG3–*x*	3, 4
	PD_PCFG4–*x*	3, 4, 6
7, 8	PD_PCFG2–*x* or PD_PCFG3–*x*	3, 4
	PD_PCFG4–*x*	3, 4, 6, 8

Pass requirements: The highest average PD power p_0 is below [$\Rightarrow P_{Class\_PD}$] for the assigned Class (pse_assigned_class).

NOTE—When pse_assigned_class is 8 and the PD uses Class 8 extended power, the highest average power may exceed the value listed in the Table.

Assigned Class	1	2	3	4	5	6	7	8
$\Rightarrow P_{Class\_PD}$ (W)	3.84	6.49	13	25.5	40	51	62	71.3

11.45 PD45 $P_{Port\_PD\text{-}2P}$ (dual-signature PD)

This test is for PICS PD45, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.2.

Requirement from IEEE Std 802.3bt™-2018
For dual-signature PDs, $P_{Port\_PD\text{-}2P}$ shall not exceed $P_{Class\_PD\text{-}2P}$ for the assigned class.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.46 PD46 Power draw for Autoclass PDs

This test is for PICS PD46, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.2.

Requirement from IEEE Std 802.3bt™-2018

A PD that has enabled Autoclass during Physical Layer classification or has requested Autoclass through DLL, shall not draw more power than $P_{Autoclass\_PD}$, unless the PD successfully negotiates a different power level, up to the PD requested Class, through Data Link Layer classification as defined in 145.5.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.47 PD47 Power consumption after DLL classification

This test is for PICS PD47, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.2.

Requirement from IEEE Std 802.3bt™-2018
Single-signature PDs that have successfully completed DLL classification shall not exceed a power consumption of PDMaxPowerValue as defined in 145.5.3.3.1.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.48 PD48 Power consumption after DLL classification

This test is for PICS PD48, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.2.

Requirement from IEEE Std 802.3bt™-2018
Dual-signature PDs that have successfully completed DLL classification shall not exceed a power consumption of PDMaxPowerValue_mode(X) on Mode X as defined in 145.5.3.4.2.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.49 PD49 Input average power exceptions for single-signature PDs

This test is for PICS PD49, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.2.1.

> Requirement from IEEE Std 802.3bt™-2018
>
> For single-signature PDs assigned to Class 8 and PDMaxPowerValue set to 713 or greater, when additional information is available to the PD regarding actual link section DC resistance between the PSE PI and the PD PI, the PD may consume greater than P_{Class_PD} but shall not consume greater than P_{Class} at the PSE PI and shall not draw a total 4-pair current in excess of 2 * I_{Cable} as defined in Table 145–1.

Last modification: Initial version.

History of changes: —

Test applicable to: Single-signature PDs with PD Logo Class 8 and Class 8 extended power

11.49.1 Test 1 — Total 4-pair current

Test setup: Connect the PSE model to the PD using the following settings:

- Power configuration PD_PCFG4–1 listed in Table 7
- psemodel_max_class is set to 8
- $R_{PSEpair n}$ set to less than 1 Ω
- V_{supply} set in the range of 52 V to 53 V

Test procedure:

1. Apply a classification, inrush, and power on waveform.
2. Wait for at least 10 s.
3. Measure the highest average value of $I_{pair\_negative}$ for at least 10 s (with a 1 second sliding window).
4. Measure the highest average input power (see 6.1.6), increased with $\sum I^2_{pair n} \times R_{PSEpair n}$ for at least 10 s and record as p_0.
5. ↻ Repeat the test using PD_PCFG4–2, PD_PCFG4–3, and PD_PCFG4–4 (see Table 7).

Pass requirements:

- $I_{pair\_negative} < 1.92 A [⇳ I_{Cable}]$
- $p_0 < 90 W$

11.49.2 Test 2 — P_{Class} power

Test setup: Connect the PSE model to the PD using the following settings:

- Power configuration PD_PCFG4–1 listed in Table 7
- psemodel_max_class is set to 8

- $R_{PSEpair n}$ set in the range of 5 Ω to 6.25 Ω
- V_{supply} set in the range of 52 V to 53 V

Test procedure:

1. Apply a classification, inrush, and power on waveform.
2. Wait for at least 10 s.
3. Measure the highest average input power (see 6.1.6), increased with $\sum I^2_{pair n} \times R_{PSEpair n}$ for at least 10 s and record as p_0.
4. ↻ Repeat the test using PD_PCFG4–2, PD_PCFG4–3, and PD_PCFG4–4 (see Table 7).

Pass requirements: $p_0 < 90$ W.

11.50 PD50 Input average power exceptions for dual-signature PDs

This test is for PICS PD50, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.2.1.

Requirement from IEEE Std 802.3bt™-2018

For dual-signature PDs assigned to Class 5 and PDMaxPowerValue_mode(X) set to 356 or greater, when additional information is available to the PD regarding actual link section DC resistance between the PSE PI and the PD PI, the PD may consume greater than $P_{Class\_PD\text{-}2P}$ but shall not consume greater than $P_{Class\text{-}2P}$ on the pairset at the PSE PI and shall not draw current in excess of I_{Cable} as defined in Table 145–1.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.51 PD51 PD input inrush current

This test is for PICS PD51, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.3.

> Requirement from IEEE Std 802.3bt™-2018
>
> PDs shall draw less than I_{Inrush_PD} and $I_{Inrush\_PD\text{-}2P}$ from T_{Inrush_PD} max until T_{delay} min, when connected to a source that meets the requirements of 145.2.10.6.

Last modification: Initial version.

History of changes: —

11.51.1 Test 1 — Low inrush (2-pair) on Mode A

Test applicable to: All single-signature PDs.

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG2–2 (see Table 7)
- psemodel_max_class set to 6

Test procedure:

1. Change S_{altA} to the "I" position and set $I_{curlimA}$ to 410 mA ± 10 mA
2. Apply a classification waveform on Mode A only
3. At $T_{Class}n$ set V_{supply} to 56 V and mark this time as t_0
4. Wait until $t_0 + 50$ ms.
5. At $t_0 + 50$ ms change S_{altA} from “I” to “R”
6. Measure $I_{pair\_negative\_A}$ from $t_0 + 50$ ms to $t_0 + 80$ ms.
7. ↻ Repeat the test with psemodel_max_class set to 4 and 3.

Pass requirements: Either:

1. V_{PDPI_A} does not fall below 30 V after rising above 30 V for the first time
2. The measured current $I_{pair\_negative\_A}$ is less than 400 mA [⇩I_{Inrush_PD}] during the measurement period defined in step 6.
3. The highest instantaneous power is less than ⇩P_{Peak_PD} for the class determined by min(3, pd_req_class) during the measurement period defined in step 6.

Or:

1. Test 11.51.5 passes

11.51.2 Test 2 — Low inrush (2-pair) on Mode B

Test applicable to: All single-signature PDs.

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG2–3 (see Table 7)
- psemodel_max_class set to 6

Test procedure:

1. Change S_{altB} to the "I" position and set $I_{curlimB}$ to 410 mA ± 10 mA
2. Apply a classification waveform on Mode B only.
3. At $T_{Class}n$ set V_{supply} to 56 V. Mark this time as t_0
4. Set I_{curlim_B} per Table 44.
5. Wait until $t_0 + 50$ ms.
6. At $t_0 + 50$ ms change S_{altB} from “I” to “R”.
7. Measure $I_{pair\_negative\_B}$ from $t_0 + 50$ ms to $t_0 + 80$ ms.
8. ↻ Repeat the test with psemodel_max_class set to 4 and 3.

Pass requirements: Either:

1. V_{PDPI_B} does not fall below 30 V after rising above 30 V for the first time
2. The measured current $I_{pair\_negative\_B}$ is less than 400 mA [⇩I_{Inrush_PD}] during the measurement period defined in step 6.
3. The highest instantaneous power is less than ⇩P_{Peak_PD} for the class determined by min(3, pd_req_class) during the measurement period defined in step 6.

Or:

1. Test 11.51.6 passes

Table 41: Current limit setting as function of V_{PSEPI_A} or V_{PSEPI_B} for PD51 (Class 1 through 6)

V_{PSEPI_A} or V_{PSEPI_B}	I_{curlim_A} or I_{curlim_B}
0 V to 10 V	5 mA to 20 mA
10 V to 30 V	60 mA to 80 mA
30 V to 57 V	400 mA to 420 mA

11.51.3 Test 3 — Low inrush (4-pair)

Test applicable to: All single-signature PDs.

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG4–2 (see Table 7)
- psemodel_max_class set to 6

Test procedure:

1. Change S_{altA} and S_{altB} to the "I" position and set I_{curlim_A} and I_{curlim_B} to 205 mA ± 5 mA each
2. Apply a classification waveform.
   NOTE—The current limit must actively track max(V_{PSEPI_A}, V_{PSEPI_B}) throughout the inrush period.
3. At Tclass_end, set V_{supply} to 56 V. Mark this time as t_0.
4. Wait until $t_0 + 50$ ms.
5. At $t_0 + 50$ ms change S_{altA} and S_{altB} from “I” to “R”.
6. Measure $I_{pair\_negative}$ from $t_0 + 50$ ms to $t_0 + 80$ ms.
7. ↻ Repeat the test with psemodel_max_class set to 4 and 3.
8. ↻ Repeat the test using power configuration PD_PCFG4–3.

Pass requirements: Either:

1. V_{PDPI_A} does not fall below 30 V after rising above 30 V for the first time
2. V_{PDPI_B} does not fall below 30 V after rising above 30 V for the first time
3. The measured current $I_{pair\_negative\_A}$ is less than 400 mA 800 mA [⇨I_{Inrush_PD}] during the measurement period defined in step 6.
4. The highest instantaneous power is less than ⇨P_{Peak_PD} for the class determined by min(3, pd_req_class) during the measurement period defined in step 6.

Or:

1. Test 11.51.7 passes

Table 42: Current limit setting as function of max(V_{PSEPI_A}, V_{PSEPI_B}) for PD51(Class 1 through 6)

max(V_{PSEPI_A}, V_{PSEPI_B})	I_{curlim_A} and I_{curlim_B}
0 V to 10 V	2.5 mA to 10 mA
10 V to 30 V	30 mA to 40 mA
30 V to 57 V	200 mA to 210 mA

11.51.4 Test 4 — High inrush

Test applicable to: Single-signature PDs with PD Logo Class 7 or 8.

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG4–2 (see Table 7)
- psemodel_max_class set to 8

Test procedure:

1. Change S_{altA} and S_{altB} to the "I" position and set I_{curlim_A} and I_{curlim_B} to 205 mA ± 5 mA each
2. Apply a classification waveform.
   NOTE—The current limit must actively track max(V_{PSEPI_A}, V_{PSEPI_B}) throughout the inrush period.
3. At Tclass_end, set V_{supply} to 56 V. Mark this time as t_0.
4. Wait until $t_0 + 50$ ms.
5. At $t_0 + 50$ ms change S_{altA} and S_{altB} from “I” to “R”.
6. Measure $I_{pair\_negative}$ from $t_0 + 50$ ms to $t_0 + 80$ ms.

Pass requirements: Either:

1. V_{PDPI_A} does not fall below 30 V after rising above 30 V for the first time
2. V_{PDPI_B} does not fall below 30 V after rising above 30 V for the first time
3. The measured current $I_{pair\_negative}$ is less than 800 mA 800 mA [⇨I_{Inrush_PD}] during the measurement period defined in step 6.
4. The highest instantaneous power is less than [⇨P_{Peak_PD}] for the class determined by min(3, pd_req_class) during the measurement period defined in step 6.

Or:

1. Test 11.51.8 passes

Table 43: Current limit setting as function of max(V_{PSEPI_A}, V_{PSEPI_B}) for PD51(Class 7 and 8)

max(V_{PSEPI_A}, V_{PSEPI_B})	I_{curlim_A} and I_{curlim_B}
0 V to 10 V	2.5 mA to 10 mA
10 V to 30 V	30 mA to 40 mA
30 V to 57 V	400 mA to 420 mA

11.51.5 Test 5 — Low inrush (2-pair) on Mode A

Test applicable to: All single-signature PDs.

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG2–2 (see Table 7)
- psemodel_max_class set to 6
- V_{supply} set in the range of 55 V to 57 V

Test procedure:

1. Apply a classification waveform on Mode A only
2. Set $I_{curlimA}$ per Table 41
3. Note: The current limit must actively track V_{PSEPI_A} throughout the inrush period
4. Change S_{altA} from "V" to "I" and mark this time as t_0
5. Wait until $t_0 + 50\,ms$.
6. At $t_0 + 50\,ms$ change S_{altA} from “I” to “R”
7. Measure $I_{pair\_negative\_A}$ from $t_0 + 50\,ms$ to $t_0 + 80\,ms$.
8. ↻ Repeat the test with psemodel_max_class set to 4 and 3.

Pass requirements: Either:

1. The measured current $I_{pair\_negative\_A}$ is less than 400 mA [⇨I_{Inrush_PD}] during the measurement period defined in step 6.
2. The highest instantaneous power is less than [⇨P_{Peak_PD}] for the class determined by min(3, pd_req_class) during the measurement period defined in step 6.

Or:

1. Test 11.51.1 passes

11.51.6 Test 6 — Low inrush (2-pair) on Mode B

Test applicable to: All single-signature PDs.

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG2–3 (see Table 7)
- psemodel_max_class set to 6
- V_{supply} set in the range of 55 V to 57 V

Test procedure:

1. Apply a classification waveform on Mode B only.
2. Set I_{curlim_B} per Table 44.
   NOTE—The current limit must actively track V_{PSEPI_B} throughout the inrush period.
3. Change S_{altB} to the "I" position and mark the time as t_0
4. Wait until $t_0 + 50\,ms$.
5. At $t_0 + 50\,ms$ change S_{altB} from “I” to “R”.
6. Measure $I_{pair\_negative\_B}$ from $t_0 + 50\,ms$ to $t_0 + 80\,ms$.
7. ↻ Repeat the test with psemodel_max_class set to 4 and 3.

Pass requirements: Either:

1. The measured current $I_{pair\_negative\_B}$ is less than 400 mA [⇨I_{Inrush_PD}] during the measurement period defined in step 6.
2. The highest instantaneous power is less than [⇨P_{Peak_PD}] for the class determined by min(3, pd_req_class) during the measurement period defined in step 6.

Or:

1. Test 11.51.2 passes

Table 44: Current limit setting as function of V_{PSEPI_A} or V_{PSEPI_B} for PD51 (Class 1 through 6)

V_{PSEPI_A} or V_{PSEPI_B}	I_{curlim_A} or I_{curlim_B}
0 V to 10 V	5 mA to 20 mA
10 V to 30 V	60 mA to 80 mA
30 V to 57 V	400 mA to 420 mA

11.51.7 Test 7 — Low inrush (4-pair)

Test applicable to: All single-signature PDs.

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG4–2 (see Table 7)
- psemodel_max_class set to 6

Test procedure:

1. Apply a classification waveform.
2. Set I_{curlim_A} and I_{curlim_B} per Table 45
   NOTE—The current limit must actively track max(V_{PSEPI_A}, V_{PSEPI_B}) throughout the inrush period.
3. Change S_{altA} and S_{altB} to the "I" position and mark the time as t_0
4. Wait until $t_0 + 50$ ms.
5. At $t_0 + 50$ ms change S_{altA} and S_{altB} from “I” to “R”.
6. Measure $I_{pair\_negative}$ from $t_0 + 50$ ms to $t_0 + 80$ ms.
7. ↻ Repeat the test with psemodel_max_class set to 4 and 3.
8. ↻ Repeat the test using power configuration PD_PCFG4–3.

Pass requirements: Either:

1. The measured current $I_{pair\_negative}$ is less than 400 mA [800 mA [⇨I_{Inrush_PD}]] during the measurement period defined in step 6.
2. The highest instantaneous power is less than [⇨P_{Peak_PD}] for the class determined by min(3, pd_req_class) during the measurement period defined in step 6.

Or:

1. Test 11.51.3 passes

Table 45: Current limit setting as function of max(V_{PSEPI_A}, V_{PSEPI_B}) for PD51(Class 1 through 6)

max(V_{PSEPI_A}, V_{PSEPI_B})	I_{curlim_A} and I_{curlim_B}
0 V to 10 V	2.5 mA to 10 mA
10 V to 30 V	30 mA to 40 mA
30 V to 57 V	200 mA to 210 mA

11.51.8 Test 8 — High inrush

Test applicable to: Single-signature PDs with PD Logo Class 7 or 8.

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG4–2 (see Table 7)
- psemodel_max_class set to 8
- V_{supply} set in the range of 55 V to 57 V

Test procedure:

1. Change S_{altA} and S_{altB} to the "I" position and set I_{curlim_A} and I_{curlim_B} to 205 mA ± 5 mA each
2. Apply a classification waveform.

   NOTE—The current limit must actively track max(V_{PSEPI_A}, V_{PSEPI_B}) throughout the inrush period.
3. At Tclass_end, set V_{supply} to 56 V. Mark this time as t_0.
4. Wait until $t_0 + 50$ ms.
5. At $t_0 + 50$ ms change S_{altA} and S_{altB} from “I” to “R”.
6. Measure $I_{pair\_negative}$ from $t_0 + 50$ ms to $t_0 + 80$ ms.

Pass requirements: Either:

1. The measured current $I_{pair\_negative}$ is less than 800 mA [800 mA [⇨I_{Inrush_PD}]] during the measurement period defined in step 6.
2. The measured current $I_{pair\_negative\_A}$ and $I_{pair\_negative\_B}$ are both less than 600 mA during the measurement period defined in step 6.
3. The highest instantaneous power is less than [⇨P_{Peak_PD}] for the class determined by min(3, pd_req_class) during the measurement period defined in step 6.

Or:

1. Test 11.51.4 passes

Table 46: Current limit setting as function of max(V_{PSEPI_A}, V_{PSEPI_B}) for PD51 (Class 7 and 8)

max(V_{PSEPI_A}, V_{PSEPI_B})	I_{curlim_A} and I_{curlim_B}
0 V to 10 V	2.5 mA to 10 mA
10 V to 30 V	30 mA to 40 mA
30 V to 57 V	400 mA to 420 mA

11.52 PD52 P_{Class_PD} and P_{Peak_PD} for single-signature PDs assigned to Class 1, 2, or 3

This test is for PICS PD52, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.3.

> Requirement from IEEE Std 802.3bt™-2018
>
> Single-signature PDs assigned to Class 1, 2, or 3 shall conform to P_{Class_PD} and P_{Peak_PD} within T_{Inrush_PD} max as defined in Table 145–29.

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG2–1 (see Table 7)
- V_{supply} set to a voltage in the range of $\Rightarrow V_{Port\_PSE\text{-}2P}$ min to $\Rightarrow V_{Port\_PSE\text{-}2P}$ min + 200 mV
- psemodel_max_class is 3

Test procedure:

1. Apply a classification waveform.
2. Determine the assigned Class (pse_assigned_class).
3. Set S_{altA} to the "I" position and set I_{curlim_A} in the range of 400 mA to 420 mA.
4. Wait for 50 ms.
5. Set S_{altA} to the "R" position.
6. Measure the highest average power and the highest instantaneous power for at least 10 s.

Pass requirements:

- The highest average power is less than $\Rightarrow P_{Class\_PD}$ for pse_assigned_class
- The highest instantaneous power is less than $\Rightarrow P_{Peak\_PD}$ for pse_assigned_class

Assigned Class	1	2	3	4	5	6	7	8
$\Rightarrow P_{Class\_PD}$ (W)	3.84	6.49	13	25.5	40	51	62	71.3
$\Rightarrow P_{Peak\_PD}$ (W)	5	8.36	14.4	28.3	42	53.5	65.1	74.9

11.53 PD53 $P_{Class\_PD\text{-}2P}$ and $P_{Peak\_PD\text{-}2P}$ for dual-signature PDs assigned to Class 1, 2, or 3

This test is for PICS PD53, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.3.

Requirement from IEEE Std 802.3bt™-2018
Dual-signature PDs assigned to Class 1, 2, or 3 shall conform to $P_{Class\_PD\text{-}2P}$ and $P_{Peak\_PD\text{-}2P}$ within T_{Inrush_PD} max as defined in Table 145–29 on that pairset.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.54 PD54 Peak power

This test is for PICS PD54, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.4.

> Requirement from IEEE Std 802.3bt™-2018
>
> At any static voltage at the PI, and any PD operating condition, with the exception described in 145.3.8.4.1, the peak power for single-signature PDs shall not exceed P_{Class_PD} for more than T_{CUT} min, as defined in Table 145–16 and 5% duty cycle.

Last modification: Initial version.

History of changes: —

Test applicable to: Single-signature PDs, except those using Class 8 extended power.

Test setup: Connect the PSE model to the PD with the following settings:

- V_{supply} set to a voltage in the range of ⇩$V_{Port\_PSE\text{-}2P}$ min to ⇩$V_{Port\_PSE\text{-}2P}$ min + 200 mV
- Power configuration and psemodel_max_class set per Test 1 in Table 47

Test procedure:

1. Apply a classification, inrush, and power on waveform.
2. Wait for at least 10 s.
3. Measure the highest instantaneous power and the instantaneous power over the measurement interval for at least 10 s.
4. ↻ Repeat the procedure for each test listed in Table 47.

Table 47: Peak power test permutations

Test	Power configuration	psemodel_max_class	
Test 1	PD_PCFG4–2	8	Skip if PD Logo Class ≤ 6
Test 2	PD_PCFG4–3	8	Skip if PD Logo Class ≤ 6
Test 3	PD_PCFG4–2	6	Skip if PD Logo Class ≤ 4
Test 4	PD_PCFG4–3	6	Skip if PD Logo Class ≤ 4
Test 5	PD_PCFG4–2	4	
Test 6	PD_PCFG4–3	4	
Test 7	PD_PCFG2–1	4	Skip if PD Logo Class ≤ 3
Test 8	PD_PCFG2–3	4	Skip if PD Logo Class ≤ 3
Test 9	PD_PCFG2–1	3	
Test 10	PD_PCFG2–3	3	

Pass requirements:

- The highest instantaneous power does not exceed ⇩P_{Peak_PD} for pse_assigned_class
- In any window with a 1 second width in the instantaneous power measurements, the measured power does not exceed ⇩P_{Class_PD} for a cumulative duration longer than 50 ms

Assigned Class	1	2	3	4	5	6	7	8
➪P_{Class_PD} (W)	3.84	6.49	13	25.5	40	51	62	71.3
➪P_{Peak_PD} (W)	5	8.36	14.4	28.3	42	53.5	65.1	74.9

11.55 PD55 Peak power

This test is for PICS PD55, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.4.

Requirement from IEEE Std 802.3bt™-2018

At any static voltage at the PI, and any PD operating condition, with the exception described in 145.3.8.4.1, the peak power for a dual-signature PD shall not exceed $P_{Class\_PD\text{-}2P}$ for more than T_{CUT} min, as defined in Table 145–16 and 5% duty cycle.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.56 PD56 Peak operating power exceptions

This test is for PICS PD56, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.4.1.

Requirement from IEEE Std 802.3bt™-2018

For single-signature PDs assigned to Class 8 and for dual-signature PDs assigned to Class 5, when additional information is available to the PD regarding actual link section DC resistance between the PSE PI and the PD PI, in any operating condition with any static voltage at the PI, the peak power shall not exceed maximum P_{Port_PD} for single-signature PDs and maximum $P_{Port\_PD\text{-}2P}$ for dual-signature PDs at the PSE PI for more than T_{CUT} min, as defined in Table 145–16 and with 5% duty cycle.

Last modification: Initial version.

History of changes: —

Test applicable to: Single-signature PDs with PD Logo Class 8 extended power.

Test applicable to: No test is required.

11.57 PD57 Peak operating power limit

This test is for PICS PD57, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.4.1.

Requirement from IEEE Std 802.3bt™-2018
Peak operating power shall not exceed 1.05 * P_{Port_PD} max for single-signature PDs and shall not exceed 1.05 * $P_{Port\_PD\text{-}2P}$ max for dual-signature PDs on each pairset.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.58 PD58 Peak transient current for single-signature PDs

This test is for PICS PD58, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.5.

> Requirement from IEEE Std 802.3bt™-2018
>
> When the input voltage at the PI is static and in the range of $V_{Port\_PD\text{-}2P}$ defined by Table 145–29, the input current drawn by a single-signature PD shall not change faster than $I_{Slewrate}$ defined in Table 145–29, in either polarity.

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG4–2 (see Table 7)
- V_{supply} set to a voltage in the range of 55 V to 57 V
- psemodel_max_class is 8
- $R_{PSEpair1}$, $R_{PSEpair2}$, $R_{PSEpair3}$, and $R_{PSEpair4}$ are set to less than 1 Ω

Test procedure:

1. Apply a classification, inrush, and power on waveform.
2. Measure the current on $I_{pair\_negative\_A}$ and $I_{pair\_negative\_B}$ for at least 10 s continuously.

Pass requirements: The slew rate of $I_{pair\_negative}$ is less than or equal to 4.7 mA/µs [⇨$I_{Slewrate}$] for the entire measurement.

11.59 PD59 Peak transient current for dual-signature PDs

This test is for PICS PD59, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.5.

Requirement from IEEE Std 802.3bt™-2018
Each pairset current drawn by a dual-signature PD shall not change faster than $I_{Slewrate}$ defined in Table 145–29, in either polarity.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.60 PD60 Behavior during transients at the PSE PI

This test is for PICS PD60, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.6.

Requirement from IEEE Std 802.3bt™-2018

A PD shall continue to operate without interruption in the presence of transients:
– lasting longer than 30 µs and less than 250 µs at the PSE PI as defined in 145.2.10.3, and causing the voltage at the PD PI to fall to no less than $V_{Tran\_PD\text{-}2P}$, as defined in Table 145–29;
– lasting less than 30 µs and causing the voltage at the PD PI to fall to not less than 34 V.

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

Test applicable to: No test is required.

11.61 PD61 Transient TR1 or TR2 applied (power limit)

This test is for PICS PD61, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.6.

> Requirement from IEEE Std 802.3bt™-2018
>
> When transient TR1 or TR2 is applied, the PD shall meet the operating power limits within $T_{Transient}$, as defined in Table 145–30, referenced from when the 'final voltage' is reached at the source.

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

11.61.1 Test 1 — TR1 in 2-pair mode

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG2–2 (see Table 7)
- V_{supply} set to 50 V
- psemodel_max_class is set to 4
- $R_{PSEpair\,n}$ is set in the range of 5 Ω to 6.25 Ω

Test procedure:

1. Apply a classification, inrush, and power on waveform.
2. Determine the assigned class (pse_assigned_class).
3. Switch S_{altA} to the "I" position and set $I_{curlimA}$ V_{supply} to $[⇩I_{LIM\text{-}2P}] + 5$ mA per pse_assigned_class.
4. Wait for at least 10 s.
5. Linearly slew V_{supply} from 50 V to 56 V at a rate of change of 2.25 V/ms.
6. Mark as t_0 the moment when $⇩V_{PSE}$ exceeds 55.5 V.
7. Measure the instantaneous power continuously from t_0 onward for at least 5 s.

pse_assigned_class	1 to 3	4	5	6	7	8
$⇩I_{LIM\text{-}2P}$ (mA)	400	684	580	720	850	1005

Pass requirements:

- The highest average power consumption from $t_0 + 10\,ms[⇩T_{Transient}] + 0.25\,ms$ is equal to or below $⇩P_{Class\_PD}$ for pse_assigned_class
- The highest instantaneous power from $t_0 + 10\,ms[⇩T_{Transient}] + 0.25\,ms$ is equal to or below $⇩P_{Peak\_PD}$ for pse_assigned_class

Assigned Class	1	2	3	4	5	6	7	8
$⇩P_{Class\_PD}$ (W)	3.84	6.49	13	25.5	40	51	62	71.3

Assigned Class	1	2	3	4	5	6	7	8
⇩P_{Peak_PD} (W)	5	8.36	14.4	28.3	42	53.5	65.1	74.9

11.61.2 Test 2 — TR1 in 4-pair mode

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG4–2 (see Table 7)
- V_{supply} set to 50 V
- psemodel_max_class is set to 6
- $R_{PSEpair\,n}$ is set in the range of 5 Ω to 6.25 Ω

Test procedure:

1. Apply a classification, inrush, and power on waveform.
2. Determine the assigned class (pse_assigned_class).
3. Switch S_{altA} to the "I" position and set $I_{curlimA}$ V_{supply} to [⇩$I_{LIM\text{-}2P}$] + 5 mA per pse_assigned_class.
4. Wait for at least 10 s.
5. Linearly slew V_{supply} from 50 V to 56 V at a rate of change of 2.25 V/ms.
6. Mark as t_0 the moment when ⇩V_{PSE} exceeds 55.5 V.
7. Measure the instantaneous power continuously from t_0 onward for at least 5 s.

pse_assigned_class	1 to 3	4	5	6	7	8
⇩$I_{LIM\text{-}2P}$ (mA)	400	684	580	720	850	1005

Pass requirements:

- The highest average power consumption from t_0 + 10 ms[⇩$T_{Transient}$] + 0.25 ms is equal to or below ⇩P_{Class_PD} for pse_assigned_class
- The highest instantaneous power from t_0 + 10 ms[⇩$T_{Transient}$] + 0.25 ms is equal to or below ⇩P_{Peak_PD} for pse_assigned_class

Assigned Class	1	2	3	4	5	6	7	8
⇩P_{Class_PD} (W)	3.84	6.49	13	25.5	40	51	62	71.3

Assigned Class	1	2	3	4	5	6	7	8
⇩P_{Peak_PD} (W)	5	8.36	14.4	28.3	42	53.5	65.1	74.9

11.61.3 Test 3 — TR2 in 2-pair mode

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG2–2 (see Table 7)

- V_{supply} set to 52 V
- psemodel_max_class is set to 4
- $R_{PSEpair n}$ is set in the range of 5 Ω to 6.25 Ω

Test procedure:

1. Apply a classification, inrush, and power on waveform.
2. Determine the assigned class (pse_assigned_class).
3. Switch S_{altA} to the "I" position and set $I_{curlimA}$ V_{supply} to [⇩I_{LIM-2P}] + 5 mA per pse_assigned_class.
4. Wait for at least 10 s.
5. Linearly slew V_{supply} from 52 V to 56 V at a rate of change of 2.25 V/ms.
6. Mark as t_0 the moment when ⇩V_{PSE} exceeds 55.5 V.
7. Measure the instantaneous power continuously from t_0 onward for at least 5 s.

pse_assigned_class	1 to 3	4	5	6	7	8
⇩I_{LIM-2P} (mA)	400	684	580	720	850	1005

Pass requirements:

- The highest average power consumption from t_0 + 6 ms[⇩$T_{Transient}$] is equal to or below ⇩P_{Class_PD} for pse_assigned_class
- The highest instantaneous power from t_0 + 6 ms[⇩$T_{Transient}$] is equal to or below ⇩P_{Peak_PD} for pse_assigned_class

Assigned Class	1	2	3	4	5	6	7	8
⇩P_{Class_PD} (W)	3.84	6.49	13	25.5	40	51	62	71.3

Assigned Class	1	2	3	4	5	6	7	8
⇩P_{Peak_PD} (W)	5	8.36	14.4	28.3	42	53.5	65.1	74.9

11.61.4 Test 4 — TR2 in 4-pair mode

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG4–2 (see Table 7)
- V_{supply} set to 52 V
- psemodel_max_class is set to 6
- $R_{PSEpair n}$ is set in the range of 5 Ω to 6.25 Ω

Test procedure:

1. Apply a classification, inrush, and power on waveform.
2. Determine the assigned class (pse_assigned_class).
3. Switch S_{altA} to the "I" position and set $I_{curlimA}$ V_{supply} to [⇩I_{LIM-2P}] + 5 mA per pse_assigned_class.

4. Wait for at least 10 s.
5. Linearly slew V_{supply} from 52 V to 56 V at a rate of change of 2.25 V/ms.
6. Mark as t_0 the moment when $\Rightarrow V_{PSE}$ exceeds 55.5 V.
7. Measure the instantaneous power continuously from t_0 onward for at least 5 s.

pse_assigned_class	1 to 3	4	5	6	7	8
$\Rightarrow I_{LIM\text{-}2P}$ (mA)	400	684	580	720	850	1005

Pass requirements:

- The highest average power consumption from $t_0 + 6$ ms[$\Rightarrow T_{Transient}$] is equal to or below $\Rightarrow P_{Class\_PD}$ for pse_assigned_class
- The highest instantaneous power from $t_0 + 6$ ms[$\Rightarrow T_{Transient}$] is equal to or below $\Rightarrow P_{Peak\_PD}$ for pse_assigned_class

Assigned Class	1	2	3	4	5	6	7	8
$\Rightarrow P_{Class\_PD}$ (W)	3.84	6.49	13	25.5	40	51	62	71.3

Assigned Class	1	2	3	4	5	6	7	8
$\Rightarrow P_{Peak\_PD}$ (W)	5	8.36	14.4	28.3	42	53.5	65.1	74.9

11.62 PD62 Transient TR1 or TR2 applied (source current limit)

This test is for PICS PD62, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.6.

> Requirement from IEEE Std 802.3bt™-2018
>
> When transient TR1 or TR2 is applied, the PD shall not cause the source to be in current limit for longer than T_{LIM} min.

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

11.62.1 Test 1 — TR1 in 2-pair mode

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG2–2 (see Table 7)
- V_{supply} set to 50 V
- psemodel_max_class is set to 4
- $R_{PSEpair\,n}$ is set in the range of 5 Ω to 6.25 Ω

Test procedure:

1. Apply a classification, inrush, and power on waveform.
2. Determine the assigned class (pse_assigned_class).
3. Switch S_{altA} to the "I" position and set $I_{curlimA}$ to [⇩$I_{LIM\text{-}2P}$] + 5 mA per pse_assigned_class.
4. Wait for at least 10 s.
5. Linearly slew V_{supply} from 50 V to 56 V at a rate of change of 2.25 V/ms.
6. Mark as t_0 the moment when ⇩V_{PSE} exceeds 55.5 V.
7. Measure $I_{pair\_negative}$ continuously from t_0 onward for at least 1 s.

pse_assigned_class	1 to 3	4	5	6	7	8
⇩$I_{LIM\text{-}2P}$ (mA)	400	684	580	720	850	1005

Pass requirements: From t_0 + 10 ms[⇩$T_{Transient}$] until the end of the measurement $I_{pair\_negative}$ is less than $I_{sourcelimit}$.

11.62.2 Test 2 — TR1 in 4-pair mode

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG4–2 (see Table 7)

- V_{supply} set to 50 V
- psemodel_max_class is set to 6
- $R_{PSEpair n}$ is set in the range of 5 Ω to 6.25 Ω

Test procedure:

1. Apply a classification, inrush, and power on waveform.
2. Determine the assigned class (pse_assigned_class).
3. Switch S_{altA} to the "I" position and set $I_{curlimA}$ to [⇩I_{LIM-2P}] + 5 mA per pse_assigned_class.
4. Wait for at least 10 s.
5. Linearly slew V_{supply} from 50 V to 56 V at a rate of change of 2.25 V/ms.
6. Mark as t_0 the moment when ⇩V_{PSE} exceeds 55.5 V.
7. Measure $I_{pair\_negative}$ continuously from t_0 onward for at least 1 s.

pse_assigned_class	1 to 3	4	5	6	7	8
⇩I_{LIM-2P} (mA)	400	684	580	720	850	1005

Pass requirements: From t_0 + 10 ms[⇩$T_{Transient}$] until the end of the measurement $I_{pair\_negative}$ is less than $I_{sourcelimit}$.

11.62.3 Test 3 — TR2 in 2-pair mode

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG2–2 (see Table 7)
- V_{supply} set to 52 V
- psemodel_max_class is set to 4
- $R_{PSEpair n}$ is set in the range of 5 Ω to 6.25 Ω

Test procedure:

1. Apply a classification, inrush, and power on waveform.
2. Determine the assigned class (pse_assigned_class).
3. Switch S_{altA} to the "I" position and set $I_{curlimA}$ to [⇩I_{LIM-2P}] + 5 mA per pse_assigned_class.
4. Wait for at least 10 s.
5. Linearly slew V_{supply} from 52 V to 56 V at a rate of change of 2.25 V/ms.
6. Mark as t_0 the moment when ⇩V_{PSE} exceeds 55.5 V.
7. Measure $I_{pair\_negative}$ continuously from t_0 onward for at least 1 s.

pse_assigned_class	1 to 3	4	5	6	7	8
⇩I_{LIM-2P} (mA)	400	684	580	720	850	1005

Pass requirements: From $t_0 + 6\,ms[\Rightarrow T_{Transient}]$ until the end of the measurement $I_{pair\_negative}$ is less than $I_{sourcelimit}$.

11.62.4 Test 4 — TR2 in 4-pair mode

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG4–2 (see Table 7)
- V_{supply} set to 52 V
- psemodel_max_class is set to 6
- $R_{PSEpair\,n}$ is set in the range of 5 Ω to 6.25 Ω

Test procedure:

1. Apply a classification, inrush, and power on waveform.
2. Determine the assigned class (pse_assigned_class).
3. Switch S_{altA} to the "I" position and set $I_{curlimA}$ to $[\Rightarrow I_{LIM\text{-}2P}] + 5\,mA$ per pse_assigned_class.
4. Wait for at least 10 s.
5. Linearly slew V_{supply} from 52 V to 56 V at a rate of change of 2.25 V/ms.
6. Mark as t_0 the moment when $\Rightarrow V_{PSE}$ exceeds 55.5 V.
7. Measure $I_{pair\_negative}$ continuously from t_0 onward for at least 1 s.

pse_assigned_class	1 to 3	4	5	6	7	8
$\Rightarrow I_{LIM\text{-}2P}$ (mA)	400	684	580	720	850	1005

Pass requirements: From $t_0 + 6\,ms[\Rightarrow T_{Transient}]$ until the end of the measurement $I_{pair\_negative}$ is less than $I_{sourcelimit}$.

11.63 PD63 Transient TR3 applied

This test is for PICS PD63, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.6.

Requirement from IEEE Std 802.3bt™-2018
When transient TR3 is applied, the PD shall meet the operating power limits within 4 ms, referenced from the beginning of the TR3 transient.

Last modification: Initial version.

History of changes: —

Test applicable to: No test required.

11.64 PD64 Ripple and noise

This test is for PICS PD64, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.7.

Requirement from IEEE Std 802.3bt™-2018

The PD shall meet V_{Noise_PD}, defined in Table 145–29, the common-mode or differential pair-to-pair noise at the PD PI generated by the PD circuitry.

Last modification: Version 1.2.

History of changes:

Version 1.1 Added a high pass filter to the measurement circuit in Figure 9 to make the test insensitive to PD load changes, as well as fixed the PI pin numbering.

Version 1.2 Previous change was incorrect per comment #9 against version 1.0. Implemented different measurement circuit with high-pass filter in Figure 10. Noise now only measured between the pairs of Mode A and Mode B.

Test applicable to: All single-signature PDs.

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG4–2 (see Table 7)
- V_{supply} set to 50 V for PD Logo Class 1 through 6 and to 52 V for PD Logo Class 7 and 8
- psemodel_max_class is set to 8
- $R_{PSEpair\,n}$ is set in the range of 0 Ω to 1 Ω
- Disable the Ethernet capability of the PSE (no AC content injected by the PSE)
- Output voltage noise of the PSE model is less than 0.01 Vpp for any AC frequency up to 1 MHz
- Connect the measurement circuit shown in Figure 10 to the PI of the PD (in parallel to the connection to the PSE model). The impedance of the voltage meters must be such that the detection signature of the PD does not materially change.

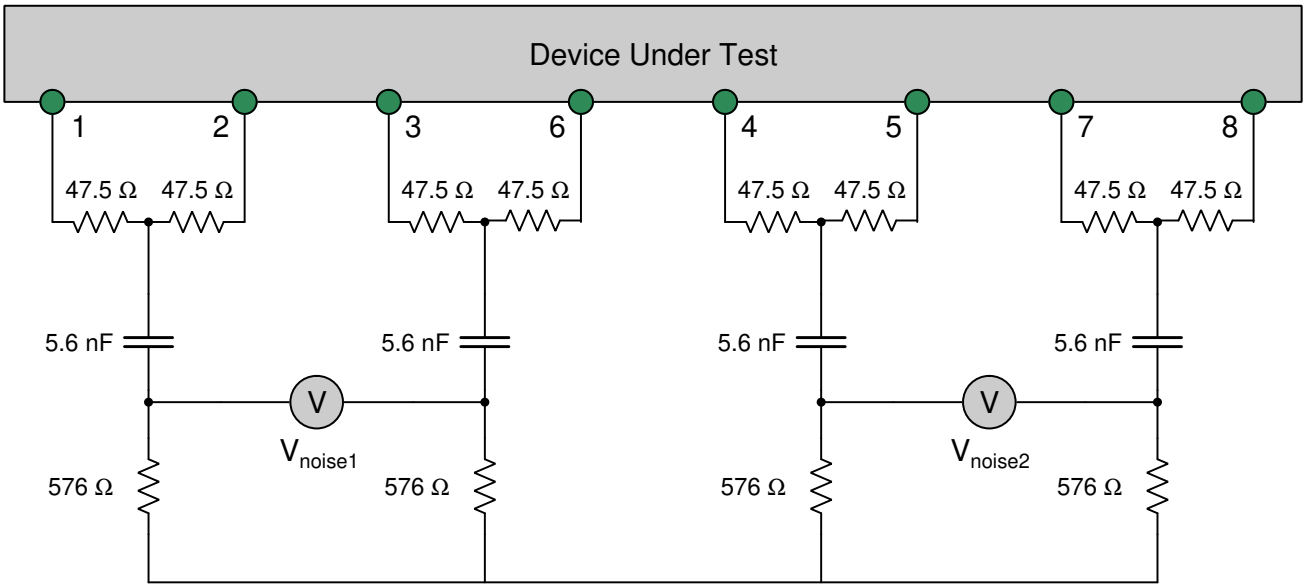

Figure 10: Pair-to-pair voltage noise measurement circuit

Test procedure:

1. Apply a classification, inrush, and power on waveform.
2. Measure the voltage peak amplitude at V_{noise1} and V_{noise2} (see Figure 10) with the measurement set to a band-limited sampling of 2 kHz over the following frequency bands:
   - 0.5 kHz to 150 kHz
   - 150 kHz to 500 kHz
   - 500 kHz to 1000 kHz
3. Let $V_{ppn} = V_{noisen} \cdot 2\sqrt{2}$
4. ↻ Repeat the measurements in step 2 with V_{supply} set in the range of 56 V to 57 V.
5. ↻ Repeat the measurements in steps 2 to 4 with $R_{PSEpairn}$ set in the range of 5 Ω to 6.25 Ω.

Pass requirements: The AC content of all of the measured pair-to-pair and pair-to-ground peak-to-peak voltages (V_{ppn}) must be equal to or below $\Rightarrow V_{noise\_PD}$.

AC band	< 500 Hz	0.5 kHz to 150 kHz	150 kHz to 500 kHz	500 kHz to 1000 kHz
$\Rightarrow V_{noise\_PD}$ (mV)pp	500	200	150	100

11.65 PD65 Ripple and noise presence

This test is for PICS PD65, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.7.

Requirement from IEEE Std 802.3bt™-2018
The PD shall operate correctly in the presence of ripple and noise generated by the PSE that appears at the PD PI.

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

Test applicable to: No test is required.

11.66 PD66 Reflected voltage (single-signature PD)

This test is for PICS PD66, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.8.

> Requirement from IEEE Std 802.3bt™-2018
>
> For a single-signature PD, when any voltage in the range of 0 V to $V_{Port\_PD\text{-}2P}$ max is applied per any of the valid 2-pair configurations, defined in Table 145–20, that have only a single pair connected to the positive potential (see Figure 145–31), the voltage on the Mode not connected to the voltage source, with a 100 kΩ resistor connected across that Mode, shall not exceed V_{refl} as defined in Table 145–29.

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

11.66.1 Test 1 — Mode A

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG2–1 (see Table 7)
- V_{supply} is set in the range of 55 V to 57 V
- psemodel_max_class is set to 8
- R_{ModeB} is set to 100 kΩ

Test procedure:

1. Apply a classification, inrush, and power on waveform on Mode A.
2. Measure V_{PDPI_B}.
3. Remove power from the PD and wait for at least the inter test wait time (see 4.4).
4. ↻ Repeat the test using power configuration PD_PCFG2–2.

Pass requirements: The measured values from V_{PDPI_B} are less than 2.8 V [ΦV_{refl}].

11.66.2 Test 2 — Mode B

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG2–3 (see Table 7)
- V_{supply} is set in the range of 55 V to 57 V
- psemodel_max_class is set to 8
- R_{ModeA} is set to 100 kΩ

Test procedure:

1. Apply a classification, inrush, and power on waveform on Mode B.
2. Measure V_{PDPI_A}.
3. Remove power from the PD and wait for at least the inter test wait time (see 4.4).
4. ↻ Repeat the test using power configuration PD_PCFG2–4.

Pass requirements: The measured values from V_{PDPI_A} are less than 2.8 V [$\Rightarrow V_{refl}$].

11.67 PD67 Reflected voltage (dual-signature PD)

This test is for PICS PD67, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.8.

Requirement from IEEE Std 802.3bt™-2018

For a dual-signature PD, when any voltage in the range of 0 V to $V_{Port\_PD\text{-}2P}$ max is applied per any of the valid 2-pair configurations, defined in Table 145–20, including those with two pairs connected to the positive potential (see Figure 145–31), the voltage on the Mode with at least one pair not connected to the voltage source, with a 100 kΩ resistor connected across that Mode, shall not exceed V_{refl} as defined in Table 145–29.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.68 PD68 Pair-to-pair current unbalance for single-signature PDs

This test is for PICS PD68, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.9.

> Requirement from IEEE Std 802.3bt™-2018
>
> Single-signature PDs shall not exceed $I_{Unbalance\_PD\text{-}2P}$ for longer than T_{CUT} min and 5% duty cycle, . . .

Last modification: Initial version.

History of changes: —

Test applicable to: Single-signature PDs with PD Logo Class 5 and greater.

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG4–1 (see Table 7)
- V_{supply} is set in the range of $\Rightarrow V_{Port\_PSE\text{-}2P}$ min + 310 mV and $\Rightarrow V_{Port\_PSE\text{-}2P}$ min + 500 mV per the assigned Class (pse_assigned_class)
- psemodel_max_class is set to 8
- $R_{PSEpair\,n}$ is set according to "Test 1" in Table 48

Test procedure:

1. Apply a classification, inrush, and power on waveform.
2. Set V_{supply} in the range of $\Rightarrow V_{Port\_PSE\text{-}2P}$ min + 310 mV and $\Rightarrow V_{Port\_PSE\text{-}2P}$ min + 500 mV per the assigned Class (pse_assigned_class).
3. Measure all pair currents, I_{pair1}, I_{pair2}, I_{pair3}, and I_{pair4} continuously, for at least 20 s after power is applied.
4. Power down the PD.
5. Wait for at least the inter-test wait time.
6. ↻ Repeat steps 1 to 5 for each Test in Table 48.
7. ↻ Repeat steps 1 to 6 using power configurations PD_PCFG4–2, PD_PCFG4–3, and PD_PCFG4–4.
8. ↻ Repeat steps 1 to 7 with psemodel_max_class set to 6. This step only applies to PDs with PD Logo Class 7 or 8.

NOTE—For PD Logo Class 5 and 6, there are 32 configurations in which 4 pair currents are measured, for PD Logo Class 7 and 8 there are 64 configurations.

Assigned Class	1 to 6	7 to 8
$\Rightarrow V_{Port\_PSE\text{-}2P}$ min (V)	50	52

Pass requirements:

The measured currents (I_{pair1}, I_{pair2}, I_{pair3}, I_{pair4}) in each step 3 are less than $\Rightarrow I_{Unbalance\_PD\text{-}2P}$ for the assigned Class (pse_assigned_class) for at least 950 ms out of any 1 s window of the measurements.

Assigned Class	5	6	7	8
$\Rightarrow I_{Unbalance\_PD\text{-}2P}$ (mA)	550	682	784	938

Table 48: $R_{PSEpair n}$ values for PD68

Test	$R_{PSEpair1}$ (Ω)	$R_{PSEpair2}$ (Ω)	$R_{PSEpair3}$ (Ω)	$R_{PSEpair4}$ (Ω)
1	0.15	0.20	0.20	0.15
2	0.15	0.20	0.15	0.20
3	0.20	0.15	0.15	0.20
4	0.20	0.15	0.20	0.15
5	5.00	5.90	5.90	5.00
6	5.00	5.90	5.00	5.90
7	5.90	5.00	5.00	5.90
8	5.90	5.00	5.90	5.00

All resistance values in this Table have a ± 1% tolerance.

11.69 PD69 Pair-to-pair peak current unbalance for single-signature PDs

This test is for PICS PD69, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.9.

> Requirement from IEEE Std 802.3bt™-2018
>
> . . . and shall not exceed $I_{Unbalance\_peak\text{-}2P}$, as defined in Table 145–31 on any pair when the PD is connected per any valid 4-pair configuration, as defined in Table 145–20, to any voltage in the range of $V_{Port\_PSE\text{-}2P}$ min + 0.31 V to $V_{Port\_PSE\text{-}2P}$ max through two common mode resistances, R_{source_min} and R_{source_max}, as defined in Equation (145–27) and shown in Figure 145–30.

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

Test setup: Connect the PSE model to the PD with the following settings:

- Power configuration PD_PCFG4–1 (see Table 7)
- V_{supply} is set in the range of ⇩$V_{Port\_PSE\text{-}2P}$ min + 310 mV and ⇩$V_{Port\_PSE\text{-}2P}$ min + 500 mV per the assigned Class (pse_assigned_class)
- psemodel_max_class is set to 8
- $R_{PSEpair\,n}$ is set according to “Test 1” in Table 48

Test procedure:

1. Apply a classification, inrush, and power on waveform.
2. Set V_{supply} in the range of ⇩$V_{Port\_PSE\text{-}2P}$ min + 310 mV and ⇩$V_{Port\_PSE\text{-}2P}$ min + 500 mV per the assigned Class (pse_assigned_class).
3. Measure all pair currents, I_{pair1}, I_{pair2}, I_{pair3}, and I_{pair4} continuously, for at least 20 s after power is applied.
4. Power down the PD.
5. Wait for at least the inter-test wait time.
6. ↻ Repeat steps 1 to 5 for each Test in Table 48.
7. ↻ Repeat steps 1 to 6 using power configurations PD_PCFG4–2, PD_PCFG4–3, and PD_PCFG4–4.
8. ↻ Repeat steps 1 to 7 with psemodel_max_class set to 6. This step only applies to PDs with PD Logo Class 7 or 8.

NOTE—For PD Logo Class 5 and 6, there are 32 configurations in which 4 pair currents are measured, for PD Logo Class 7 and 8 there are 64 configurations.

Assigned Class	1 to 6	7 to 8
⇩$V_{Port\_PSE\text{-}2P}$ min (V)	50	52

Pass requirements: The measured currents (I_{pair1}, I_{pair2}, I_{pair3}, I_{pair4}) in each step 3 are less than ⇩$I_{Unbalance\text{-}2P}$ for the assigned Class (pse_assigned_class) throughout the entire measurement.

Assigned Class	5	6	7	8
⇩$I_{Unbalance\_peak\text{-}2P}$ (mA)	578	718	848	1003

11.70 PD70 Pair-to-pair current unbalance for dual-signature PDs

This test is for PICS PD70, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.9.

Requirement from IEEE Std 802.3bt™-2018
Dual-signature PDs shall not exceed $I_{Con\_PD\text{-}2P}$, as defined in Equation (145–28), for longer than T_{CUT} min and 5% duty cycle, as defined in Table 145–16, . . .

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.71 PD71 Pair-to-pair peak current unbalance for dual-signature PDs

This test is for PICS PD71, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.8.9.

Requirement from IEEE Std 802.3bt™-2018

> . . . and shall not exceed $I_{Peak\_PD\text{-}2P}$, as defined in Equation (145–29), on any pair when the PD is connected per any valid 4-pair configuration, as defined in Table 145–20, to any voltage in the range of $V_{Port\_PSE\text{-}2P}$ min + 0.31 V to $V_{Port\_PSE\text{-}2P}$ max through two common mode resistances, R_{source_min} and R_{source_max}, as defined in Equation (145–27) and shown in Figure 145–30.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.72 PD72 PD that requires power from the PI

This test is for PICS PD72, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.9.

Requirement from IEEE Std 802.3bt™-2018
A PD that requires power from the PI shall provide a valid Maintain Power Signature (MPS) at the PI.

Last modification: Initial version.

History of changes: —

Test applicable to: All single-signature PDs.

Test applicable to: No test is required.

11.73 PD73 MPS for single-signature PDs

This test is for PICS PD73, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.9.

> Requirement from IEEE Std 802.3bt™-2018
>
> For single-signature PDs the MPS shall consist of current draw equal to or above I_{Port_MPS} for a minimum duration of T_{MPS_PD} followed by an optional MPS dropout for no longer than T_{MPDO_PD}.

Last modification: Initial version.

History of changes: —

11.73.1 Test 1 — Long MPS, Class 1 through 4

Test applicable to: All single-signature PDs.

Test setup: Connect the PSE model to the PD with the following settings:

- V_{supply} set to a voltage in the range of ⇩$V_{Port\_PSE\text{-}2P}$ min to ⇩$V_{Port\_PSE\text{-}2P}$ min + 200 mV
- Power configuration set to PD_PCFG2–2
- $R_{PSEpair1}$, $R_{PSEpair2}$, $R_{PSEpair3}$, and $R_{PSEpair4}$ are set in the range of 5 Ω to 6.25 Ω
- psemodel_max_class is set to 4
- T_{Class1} is set in the range of 10 ms to 75.5 ms [⇩T_{LCE_PD} min]

Test procedure:

1. Apply a classification, inrush, and power on waveform.
2. Wait at least 10 s.
3. Measure $I_{pair\_negative}$ for at least 5 s.

Pass requirements:

During any window of 325 ms [⇩T_{MPS_PD} + ⇩T_{MPDO_PD}], $I_{pair\_negative}$ exceeds 10 mA [⇩I_{Port_MPS}] continuously for at least 75 ms [⇩T_{MPS_PD}].

11.73.2 Test 2 — Short MPS, Class 1 through 4

Test applicable to: All single-signature PDs.

Test setup: Connect the PSE model to the PD with the following settings:

- V_{supply} set to a voltage in the range of ⇩$V_{Port\_PSE\text{-}2P}$ min to ⇩$V_{Port\_PSE\text{-}2P}$ min + 200 mV
- Power configuration set to PD_PCFG3–2
- $R_{PSEpair1}$, $R_{PSEpair2}$, $R_{PSEpair3}$, and $R_{PSEpair4}$ are set in the range of 5 Ω to 6.25 Ω
- psemodel_max_class is set to 4
- T_{Class1} is set greater than ⇩T_{LCE_PD} max

Test procedure:

1. Apply a classification, inrush, and power on waveform.
2. Wait at least 10 s.
3. Measure $I_{pair\_negative}$ for at least 5 s.
4. ↻ Repeat the test at least once using any of the PD_PCFG4–*x* power configurations.

Pass requirements:

During any window of 317 ms [⇩T_{MPS_PD} + ⇩T_{MPDO_PD}], $I_{pair\_negative}$ exceeds 10 mA [⇩I_{Port_MPS}] continuously for at least 7 ms [⇩T_{MPS_PD}].

11.73.3 Test 3 — Short MPS, Class 5 through 8

Test applicable to: Single-signature PDs with PD Logo Class 5 or greater.

Test setup: Connect the PSE model to the PD with the following settings:

- V_{supply} set to a voltage in the range of ⇩$V_{Port\_PSE\text{-}2P}$ min to ⇩$V_{Port\_PSE\text{-}2P}$ min + 200 mV
- Power configuration set to PD_PCFG4–2
- $R_{PSEpair1}$, $R_{PSEpair2}$, $R_{PSEpair3}$, and $R_{PSEpair4}$ are set in the range of 5 Ω to 6.25 Ω
- psemodel_max_class is set to 8
- T_{Class1} is set greater than ⇩T_{LCE_PD} max

Test procedure:

1. Apply a classification, inrush, and power on waveform.
2. Wait at least 10 s.
3. Measure $I_{pair\_negative}$ for at least 5 s.

Pass requirements:

During any window of 317 ms [⇩T_{MPS_PD} + ⇩T_{MPDO_PD}], $I_{pair\_negative}$ exceeds 16 mA [⇩I_{Port_MPS}] continuously for at least 7 ms [⇩T_{MPS_PD}].

11.74 PD74 I_{Port_MPS} value for single-signature PDs assigned Class 1 to 4

This test is for PICS PD74, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.9.

Requirement from IEEE Std 802.3bt™-2018
A single-signature PD shall use the I_{Port_MPS} value associated with assigned Class 1 to 4 when pse_assigned_class is 1, 2, 3, or 4, and MirroredPSEAllocatedPowerValue and PDRequestedPowerValue are less or equal to 255

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.75 PD75 I_{Port_MPS} value for single-signature PDs assigned Class 5 to 8

This test is for PICS PD75, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.9.

Requirement from IEEE Std 802.3bt™-2018
A single-signature PD shall use the I_{Port_MPS} value associated with assigned Class 5 to 8 when pse_assigned_class is 5, 6, 7, or 8, or when PDRequestedPowerValue is in the range of 256 to 999

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.76 PD76 I_{Port_MPS} value when using DLL Autoclass

This test is for PICS PD76, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.9.

Requirement from IEEE Std 802.3bt™-2018
When PDRequestedPowerValue or PSEAllocatedPowerValue is equal to 0xACAC, the PD shall use the I_{Port_MPS} value associated with the assigned Class.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.77 PD77 MPS for dual-signature PDs on each pairset independently

This test is for PICS PD77, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.9.

Requirement from IEEE Std 802.3bt™-2018

For dual-signature PDs the MPS shall consist of current draw equal to or above $I_{Port\_MPS\text{-}2P}$ on each powered pairset independently for a minimum duration of T_{MPS_PD} followed by an optional MPS dropout for no longer than T_{MPDO_PD}.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.78 PD78 Input impedance for PDs connected to Type 1 or Type 2 PSEs

This test is for PICS PD78, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.9.

Requirement from IEEE Std 802.3bt™-2018
A PD connected to a Type 1 or Type 2 PSE, shall also present input impedance with resistive and capacitive components defined in Table 145–33.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.79 PD79 T_{MPS_PD} and T_{MPDO_PD}

This test is for PICS PD79, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.9.

Requirement from IEEE Std 802.3bt™-2018
A PD shall meet the T_{MPS_PD} and T_{MPDO_PD} requirements with any series resistance in the range of R_{Chan} max between the PD PI and the source.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.80 PD80 Powered PDs that no longer require power, and identify the PSE as Type 1 or Type 2

This test is for PICS PD80, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.9.

Requirement from IEEE Std 802.3bt™-2018

Powered PDs that no longer require power, and identify the PSE as Type 1 or Type 2, shall remove both the current draw and impedance components of the MPS.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

11.81 PD81 Powered PDs that no longer require power, and identify the PSE as Type 3 or Type 4

This test is for PICS PD81, the matching requirement is located in IEEE Std 802.3bt™-2018 subclause 145.3.9.

Requirement from IEEE Std 802.3bt™-2018

Powered PDs that no longer require power, and identify the PSE as Type 3 or Type 4, shall remove the current draw component and may remove the impedance components of the MPS.

Last modification: Initial version.

History of changes: —

Test applicable to: No test is required.

12 Single-signature PD DLL Test suite

The following tests are based on the requirements in IEEE Std 802.3bt™-2018 Clause 145.5 and Clause 79.

12.1 PD DLL Test 1 Sending an updated LLDPDU

This test checks whether the PD sends out an updated LLDPDU after a change is made to the PSE allocated power field. This also serves to check if DLL is enabled within 5 minutes of startup.

Last modification: Initial version.

History of changes: —

Test applicable to: Single-signature PDs that indicate DLL capability.

Test setup: Connect the PSE model to the PD with psemodel_max_class set to 3.

Test procedure:

1. Apply a classification, inrush, and power on waveform as described in Section 7.
2. Wait until the Ethernet link is established and mark this moment as t_0.
3. Wait for 5 minutes.
4. Send a Power via MDI LLDP frame. Label this frame1.
5. Wait for 10 s.
6. Send an a Power via MDI LLDP frame with PSE allocated power value set to 'frame1.PSE allocated power value' + 1. Label this frame2.
7. Mark the time as t_1.
8. Receive Power via MDI LLDP frames until $t_1 + 10$ s. Label the last received frame as frame3.

Pass requirements:

- All received Power via MDI frames meet the requirements in Section 8.3.2.
- 'frame3.PSE allocated power value' equals 'frame2.PSE allocated power value' sent out in step 6.

12.2 PD DLL Test 2 PD DLL Power Update

This test checks for the PD to send an LLDPDU containing a Power via MDI TLV with an updated value for the 'PD requested power value' field within 10 seconds of receiving an LLDPDU containing a Power via MDI TL V where the 'PSE allocated power value' field is different from the previously communicated value.

Last modification: Initial version.

History of changes: —

Test applicable to: Single-signature PDs that indicate DLL capability.

Test setup:

- Connect the PSE model to the PD
- If the PD Logo Class is 4 or greater, set psemodel_max_class to a value less than the PD Logo Class
- If the PD Logo Class is 3 or smaller, set psemodel_max_class is set to 3

Test procedure:

1. Apply a classification, inrush, and power on waveform as described in Section 7.
2. Wait for an Ethernet link to be established.
3. Wait for 5 minutes.
4. Send a Power via MDI LLDP frame with initialized power values according to the assigned Class.
5. Wait for up to 5 minutes until a Power via MDI LLDP frame with initialized power values is received from the PD. Label this frame1.
6. Send a Power via MDI LLDP frame where
   - PD requested power value equals 'frame1.PD requested power value'
   - PSE allocated power value equals 'frame1.PSE allocated power value'

   Label this frame2.
7. Receive Power via MDI LLDP frames until either:
   - a frame is received where the PD requested power value field is greater than 'frame1.PD requested power value'
   - 30 seconds have passed

   Label this frame3.
8. After 2 minutes, if the PD does not send a higher PD requested power value then stop test (pass requirements do not apply), otherwise continue.
9. Send a Power via MDI LLDP frame where
   - PD requested power value equals 'frame3.PD requested power value'
   - PSE allocated power value equals 'frame3.PD requested power value'

   Label as frame4.
10. Receive Power via MDI LLDP frames until either:
    - a frame is received from the PD where the PSE allocated power value field equals 'frame4.PSE allocated power value'
    - 30 seconds have passed

Label this frame5. Mark as t_0 the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.

Pass requirements:

- All received Power via MDI frames meet the requirements in Section 8.3.2
- 'frame5.PSE allocated power value' equals 'frame4.PSE allocated power value'
- 'frame3.PD requested power value' is in the range for the PD's Logo Class as listed in Table 49.
- $t_0 < 10\,s$

Table 49: PD Requested power value range as function of the PD Logo Class

PD Logo Class	⇒	PD Requested Power value range
1		≤ 39
2		≤ 65
3		≤ 130
4		≤ 255
5		≤ 400
6		≤ 510
7		≤ 620
8		≤ 999

12.3 PD DLL Test 3 12 Octet Power via MDI TLV

This test checks the PD does not discard 12 octet Power Via MDI TLVs.

Last modification: Initial version.

History of changes: —

Test applicable to: Single-signature PDs that indicate DLL capability.

Test setup: Connect the PSE model to the PD.

Test procedure:

1. Apply a classification, inrush, and power on waveform as described in 6.1.4 with psemodel_max_class set to 3.
2. Wait for an Ethernet link to be established.
3. Wait for 5 minutes.
4. Send a Power via MDI LLDP frame with initialized power values corresponding to the assigned Class. Label this frame1.
5. Receive Power via MDI LLDP frames until either:
   - a frame with initialized power values is received from the PD. Label this frame2. Mark as t_0, the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.
   - 5 minutes have passed

   Label this frame2. Mark as t_0 the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.
6. Send a Power via MDI LLDP frame with the information string length field = 12 octets and the PSE allocated power value field set in the range of 131 to 255. Label this frame3.
7. Receive Power via MDI LLDP frames until either:
   - a frame is received where the PSE allocated power value field equals ‘frame3.PSE allocated power value’
   - 30 seconds have passed

   Label this frame4. Mark as t_1 the amount of time between the beginning of this step and the reception of an LLDP frame with the listed properties.

Pass requirements:

- All received Power via MDI frames meet the requirements in Section 8.3.2
- All PD transmitted TLV information string length = 29 octets or 12 octets.
- ‘frame4.PSE allocated power value’ equals ‘frame3.PSE allocated power value’.
- $t_0 < 5\,\text{min}$
- $t_1 < 10\,\text{s}$

12.4 PD DLL Test 4 Autoclass

This test verifies the PD's handling of the DLL Autoclass procedure.

Last modification: Initial version.

History of changes: —

Test applicable to: Single-signature PDs that indicate DLL capability.

Test setup: Connect the PSE model to the PD with the following settings:

- psemodel_max_class is set to the PD Logo Class
- The PSE Autoclass support bit is set

Test procedure:

1. Apply a classification, inrush, and power on waveform as described in 6.1.4.
2. Wait for an Ethernet link to be established.
3. Wait for 5 minutes.
4. Send a Power via MDI LLDP frame with initialized power values corresponding to the assigned Class. The PSE Autoclass support bit is set, and PSE allocated power value and PD requested power value are set according to the assigned Class and Table 21 and Table 24. Label this frame1.
5. Receive Power via MDI LLDP frames until either:
   - a frame with initialized power values is received from the PD and the Autoclass request bit is set. Label this frame2.
   - 5 minutes have passed. If no such frame arrives, the test is concluded and teh pass requirements do not apply. have passed

   Label this frame1. If no such frame arrives, the test is concluded and the pass requirements do not apply.
6. Wait for 10 seconds.
7. Send a Power via MDI LLDP frame with
   - PSE Autoclass completed bit set
   - PSE allocated power value set to 0xACAC

   Label this as frame frame3.
8. Receive Power via MDI LLDP frames until either:
   - a frame is received from the PD with the Autoclass request bit not set
   - 2 minutes have passed

   Label this as frame4.
9. Send a Power via MDI frame with
   - PSE Autoclass completed bit not set
   - PSE allocated power value and PD requested power value set to 0xACAC

   Label this as frame5.

Pass requirements:

- All received Power via MDI frames meet the requirements in Section 8.3.2
- If class_sig_auto is 0 (indicating the PD requests Autoclass through Physical Layer classification), 'frame2.PD requested power value' equals 0xACAC
- 'frame4.Autoclass request' bit is not set