

Ethernet in the Future: The Applications & Technologies to Enable 200 Gbps Signaling and 1.6 Tb/s Ethernet

Moderator: Mike Klempa, Alphawave Semi

Panelist: Gary Bernstein, The Siemon Company

Panelist: Kent Lusted, Intel Corporation

Panelist: Nathan Tracy, TE Connectivity

Panelist: Tony Chan Carusone, Alphawave Semi

Panelist: John Calvin, Keysight Technologies



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Presentation Disclaimer

The views expressed in this panel presentation are those of the presenters and not of the Ethernet Alliance.

About Ethernet Alliance



Mike Klempa, Product Marketing Specialist Alphawave Semi

Michael Klempa is a Product Marketing Specialist at Alphawave Semi for high-speed applications such as 112G and 224G CEI and Ethernet, and Gen6 and Gen7 PCIe. He is currently serving as the Optical Internetworking-Forum's (OIF) Physical & Link Layer Interoperability Working Group Chair. He contributes to the 802.3 Working Group, including editing the 802.3bz specification. Previously he was an Electrical Engineer at Amphenol ICC designing 400G+ Optics and Technical Manager at the University of New Hampshire InterOperability Laboratory (UNH-IOL). He obtained his Bachelors of Science in Electrical Engineering in 2013 and his Masters in Electrical Engineering in 2017.



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The Ethernet Alliance

Global Community of End Users, System Vendors, Component Suppliers & Academia

Our Mission

- **To promote** industry awareness, acceptance and advancement of technology and products based on, or dependent upon, both **existing and emerging IEEE 802 Ethernet standards** and their management.
- **To accelerate industry adoption** and remove barriers to market entry by providing a cohesive, market-responsive, industry voice.
- Provide resources to establish and **demonstrate multi-vendor interoperability**.



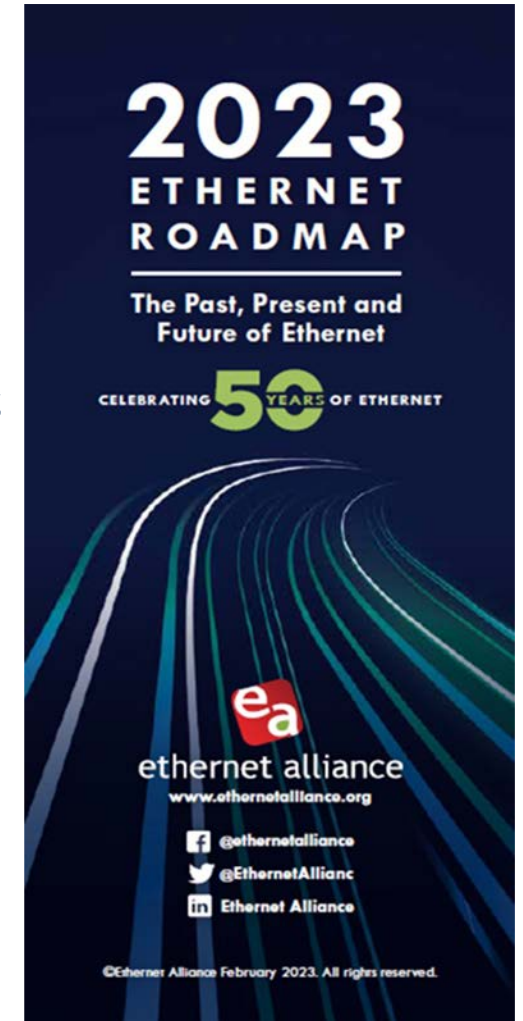
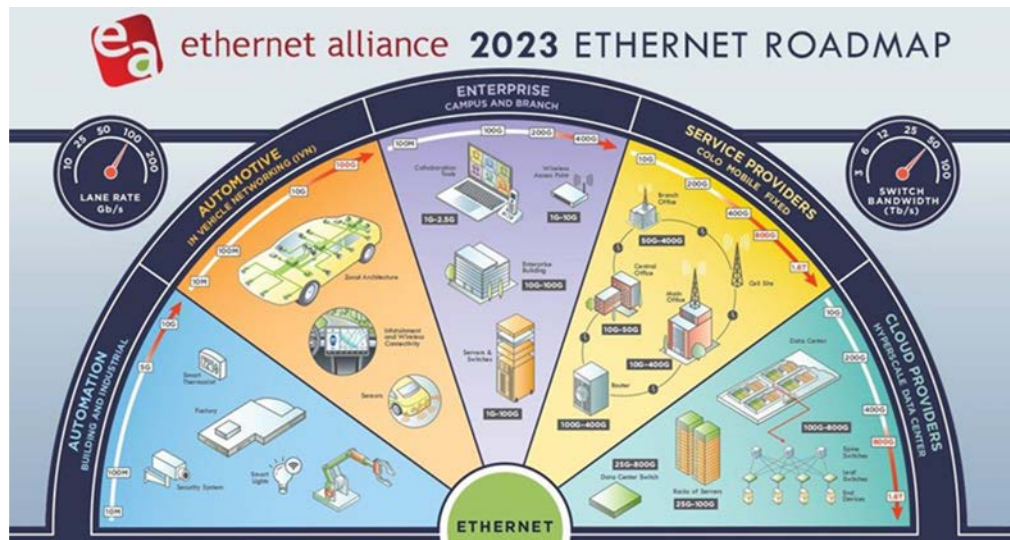
Ethernet Alliance Strategy

Expanding the Ethernet Ecosystem, Supporting Ethernet Development

- **Facilitate interoperability testing & assurance**
 - Industry Plug fests supporting member and technology initiatives
 - PoE Certification Program
- **Global outreach and collaborative interaction with other industry organizations**
 - Worldwide Membership
 - Multiple SIGs, applications and MSAs
 - Industry consensus building
- **Thought Leadership**
 - EA-hosted Technology Exploration Forums (TEFs)
 - Technology and standards incubation
- **Promotion of Ethernet**
 - Media and industry analysts outreach
 - Education
 - Marketing (trade shows & panel presentations, white papers, blogs & social media)

2023 Ethernet Roadmap

- **Digital copies & graphics** published via Alliance's [website](#)
- **Print copies** available at OFC 2023 and other events this year
- Included in the “**Ethernet Alliance in the Box**” for members
- Digital version **regularly updated** to capture latest advancements



Market Drivers



Gary Bernstein, Sr. Director of Global Data Center Sales Siemon

Gary Bernstein is the Sr. Director of Global Data Center Sales at Siemon with more than 25 years of industry experience and extensive knowledge in data center infrastructure, telecommunications, and copper and fiber structured cabling systems. Gary has had held positions in engineering, sales, product management, marketing and corporate management throughout his career. Gary has been a member of the TIA TR42.7 Copper Cabling Committee, TIA TR42.11 Optical Fiber Committee and various IEEE802.3 task forces and study groups including 40/100G "ba", 50/100/200G "cd", 200/400G "bs" Task Force and Beyond 400G. Gary has spoken on Data Center Cabling at several industry events in North America, Europe, LATAM & APAC including 7x24, AFCOM , BICSI, Cisco Live, Datacenter Dynamics and has authored several articles in industry trade publications. Gary received a Bachelor of Sciences in Mechanical Engineering from Arizona State University, is an RCDD with BICSI and a Certified Data Center Designer (CDCD) with Datacenter Dynamics.



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Top Trends Driving the Need for 800G & 1.6T

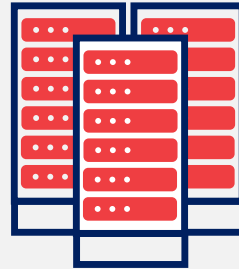
1 | CLOUD GROWTH

- Traffic within DCs projected to quadruple in 3 years
- 200G/400G compute with 800G interconnect



2 | DC OPTIMIZATION

- Flat topologies for Increased East-West traffic
- Systems with mix of 25GE to 400GE speeds
- Advancing distributed memory & storage efficiencies



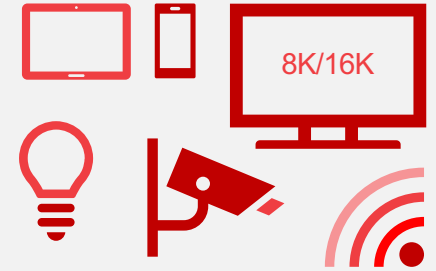
4 | HIGH SPEED I/O NICs IN DATA CENTERS

- Servers moving from 25G to 50, 100G & 200G
- Generative AI workloads on GPUs are at 100G, 200G and moving to 400G



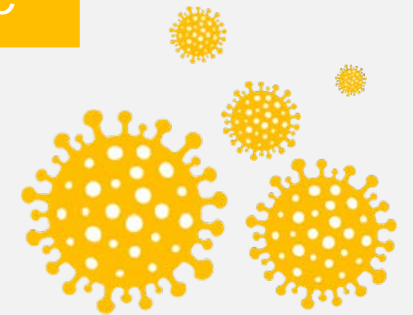
3 | BANDWIDTH-INTENSE APPLICATIONS

- Uncompressed 8K/16K high resolution video
- IoT / 5G
- Inter-pod/DCI connections
- Gaming



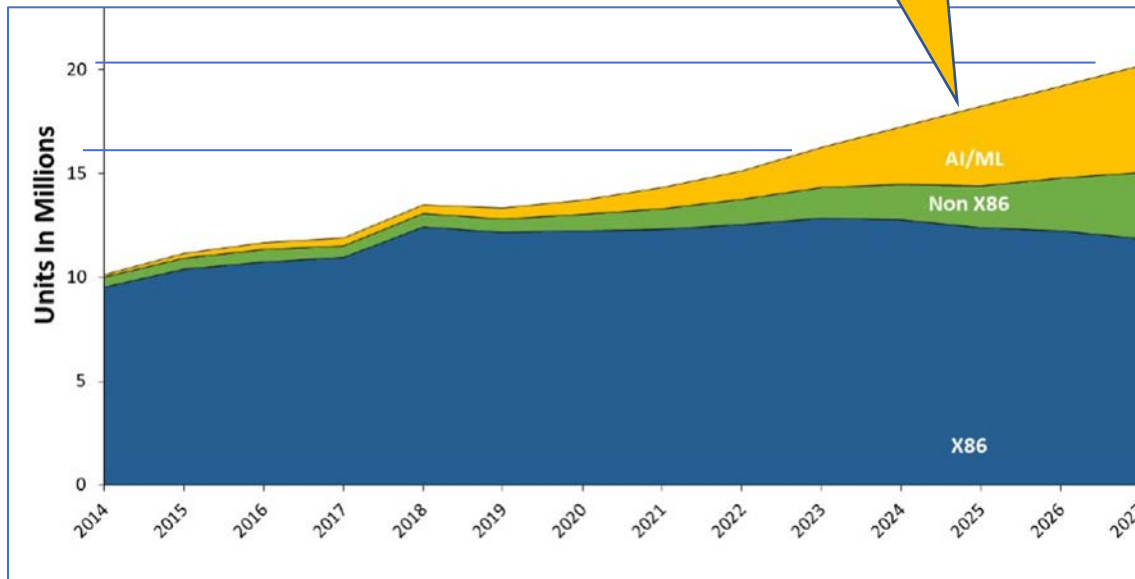
5 | COVID-19 PANDEMIC

- Remote working
- Travel restrictions
- More video traffic (Zoom, MS Teams)



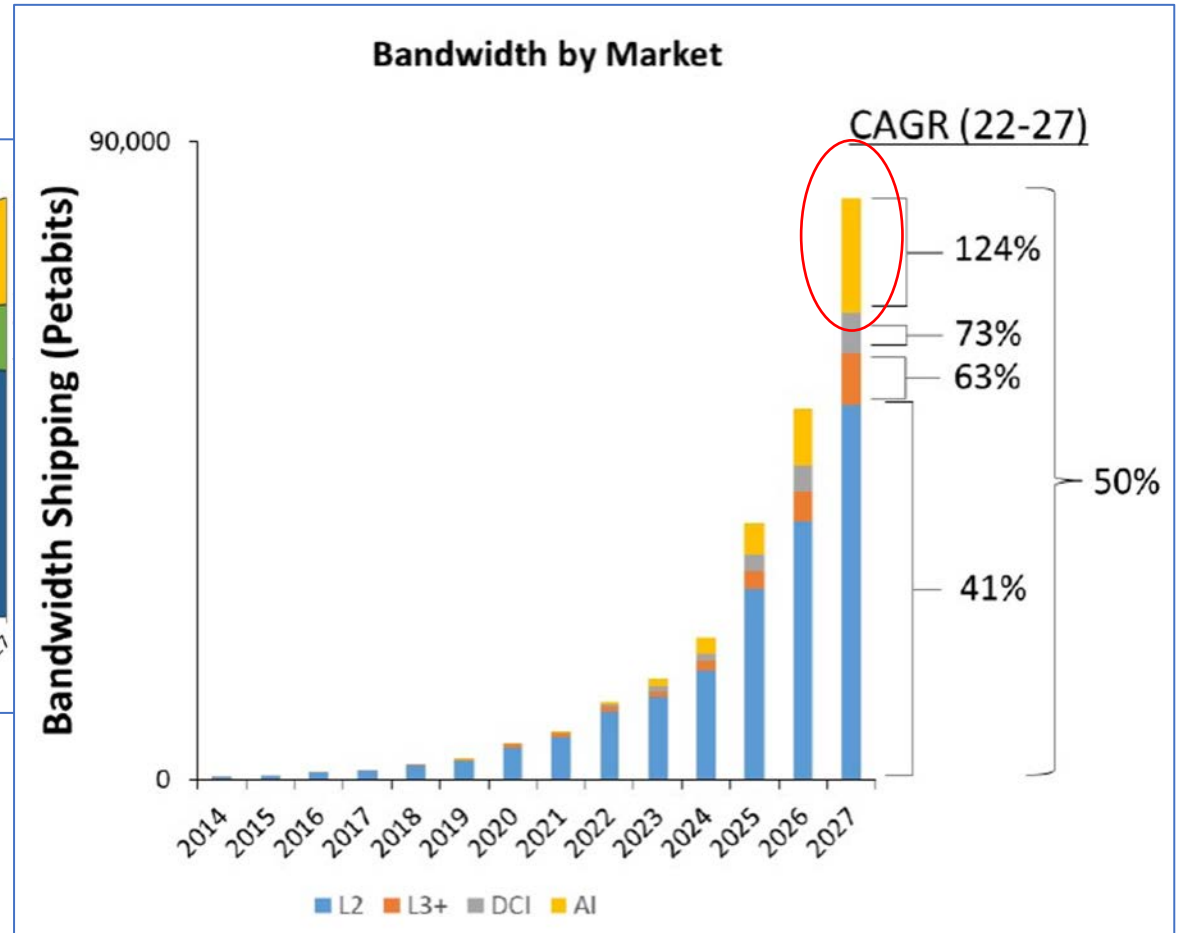
Generative AI Deeper Dive...Market Forecast

Server Shipments

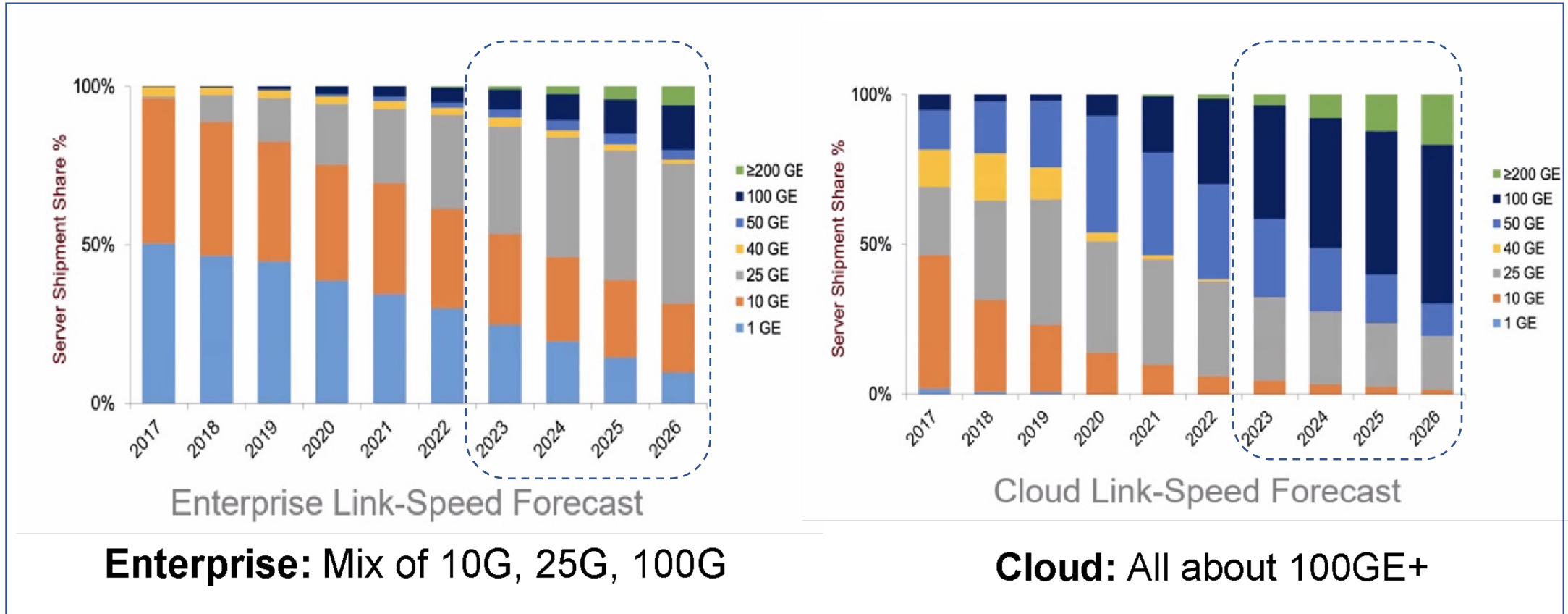


Source: 650 Group, July 2023

Bandwidth by Market



Server Speed Trends & Forecast



Source: : Dell'Oro Group, December 2022

Hyperscalers Need for 102.4T Switches

Availability of Switch Systems	2019/2020	2021	2022	2023/2024	2025/2026
Switch (Tb/s)	12.8Tbps	25.6Tbps	25.6Tbps	51.2 Tbps	102.4 Tbps
Electrical I/O (Gb/s)	50G-PAM4	50G-PAM4	100G-PAM4	100G-PAM4	200G-PAM4
Google	32x400G-OSFP (2x200G)	N/A	32x800G-OSFP (2x400G)	N/A	64x1600G-OSFP?
Amazon	32x400G-QSFP-DD (4x100G)	N/A	N/A	64x800G-OSFP (2x400G)?	64x1600G-OSFP (2x800G)?
Microsoft*	32x400G*-QSFP-DD (2023/2024)	N/A	32x800G-OSFP/QSFP-DD?? (2x400G) (Beyond 2025)	TBD	TBD
Meta*	128x100G-QSFP28	128x200G-QSFP56	N/A	64x800G-OSFP (2x400G)	TBD

Source: : Dell'Oro Group, November 2022

Ethernet Spec Development & Key Trends for 1.6TbE



Kent Lusted, Principal Engineer Intel Corporation, Ethernet PHY Standards Advisor

Kent Lusted is a Principal Engineer within Intel's Network Edge Group. He won an Intel Achievement Award in 2002 for delivering the world's first Gigabit Ethernet controllers. Since 2012, he has been an active contributor and member of the IEEE 802.3 leadership team. Kent currently is the Electrical track Chair of both the IEEE P802.3df 400 Gb/s and 800 Gb/s Ethernet Task Force and the P802.3dj 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet Task Force. Outside of work, he enjoys time with his family, playing in the snow, and exploring rural America.



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Per the IEEE SA Standards Board Operations Manual:

“At lectures, symposia, seminars, or educational courses, an individual presenting information on IEEE standards shall make it clear that the presenter’s views should be considered the personal views of that individual rather than the formal position of IEEE, IEEE SA, the Standards Committee, or the Working Group. ”

IEEE 802.3 Spec Development Overview

IEEE 802.3 defines Wired Ethernet Physical Layers

Mission: Establish, as technical standards, norms or requirements as formal documents that determine uniform criteria, method, processes, and practices for interoperability

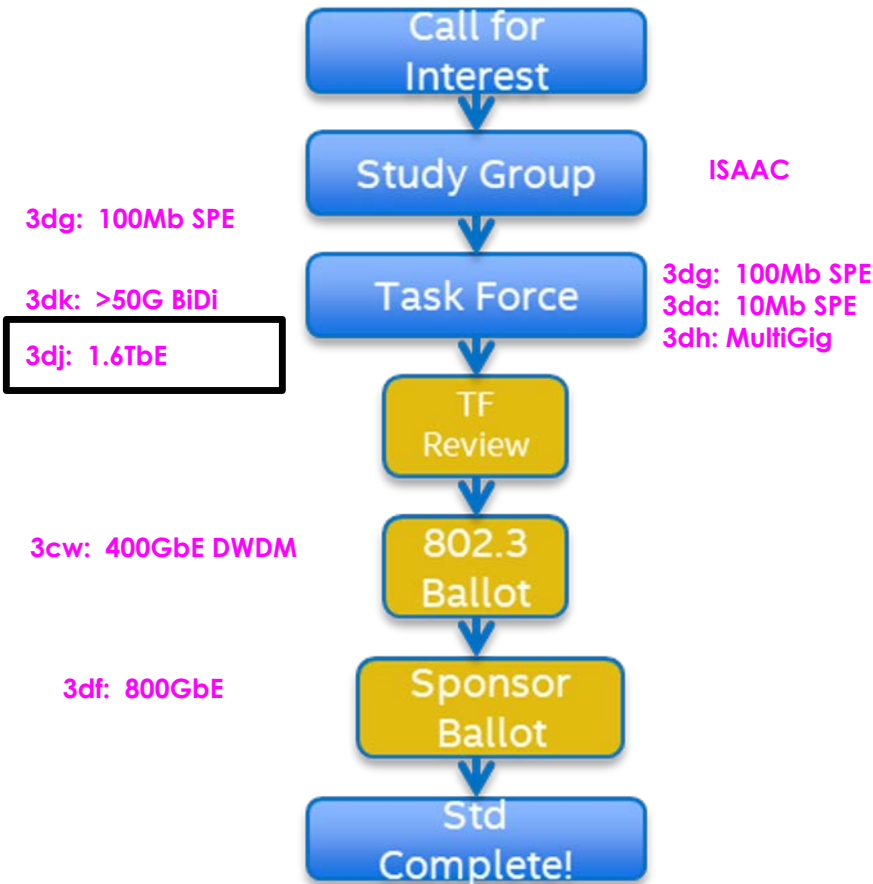
~280 members from >75 affiliations

Explore an idea

Determine the requirements

Do the work and write the spec

All done!



A Few Non-IEEE Ethernet PHY Adjacencies

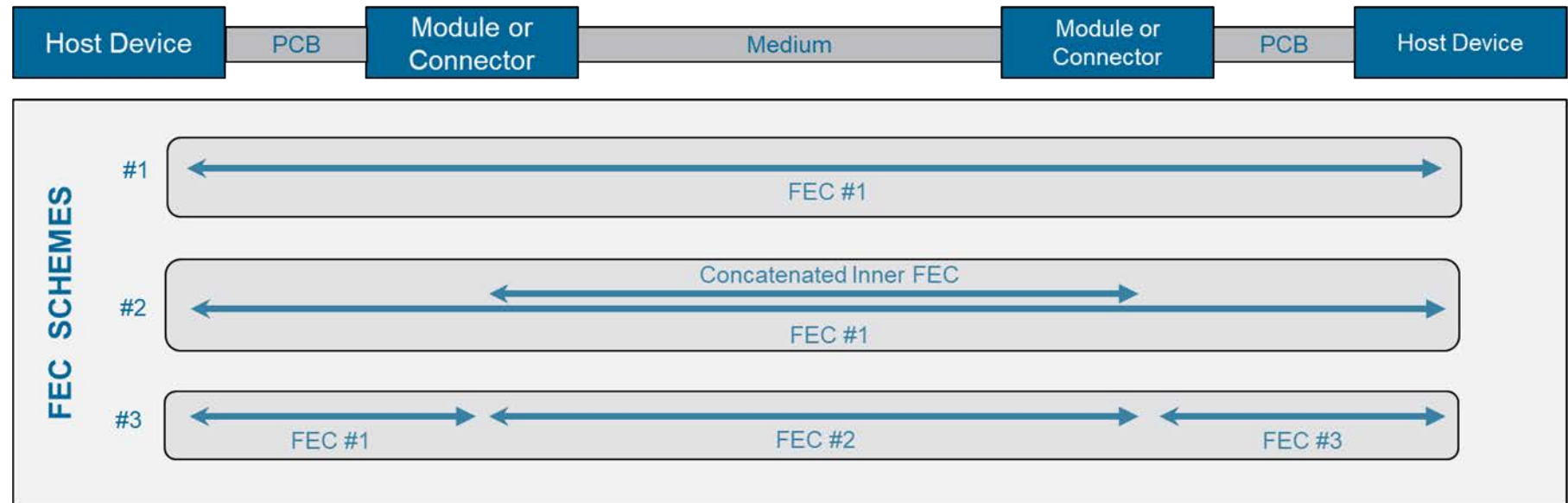
Industry Body	Mission	Noteworthy Developments
OIF	Developing interoperable electrical, optical and control solutions for an open network world	CEI-112G, CEI-224G, CPO, Linear, Coherent, CMIS
ETC	Developed specs to meet demands of Data Center Networks	LL-FEC, 8-lane 800GbE
SNIA SFF	Defines pluggable memory maps and connectors	Module Mgmt Code Tables, SFP+, QSFP
UEC	Developing an Ethernet-based architecture optimized for AI & HPC	Coming soon!

Key Trends for 200 Gbps/lane and 1.6TbE

Trend	Notes
Shift from Analog -> DSP-based SERDES	Unleashing new performance and features (e.g. MLSE)
Challenging passive copper cable reaches	Flexible host architectures enable longer reach cables. More AECs, AOCs, etc.
Multiple host port types (optic only vs. combo)	Optics on all ports; DAC on some (or need retimers). More measurement methods
More use cases with divergent latency sensitivities (AI/HPC vs. LAN vs. WAN)	New FEC architectures (concatenated or segmented) and FEC modes (FECi, FECo)

Proliferation of FEC Schemes

FEC scheme chosen for the desired medium type, reach and customer use case



Type 1: "End-to-end"

e.g.

800GBASE-CR4

Type 2: "Concatenated"

e.g.

800GBASE-FR4

Type 3: "Segmented"

e.g.

400GBASE-ZR

PHY/FEC type nomenclature per https://www.ieee802.org/3/dj/public/23_03/brown_3dj_01a_2303.pdf

Credit: John D'Ambrosia

Nomenclature By Rate and Medium Type

Ethernet Rate	Assumed Signaling Rate	AUI	Backplane	Cu Cable	SMF 500m	SMF 2km	SMF 10km	SMF 40km
200 Gb/s	200 Gb/s	200GAUI-1 C2C C2M	200GBASE-KR1	200GBASE-CR1	200GBASE-DR1	200GBASE-FR1		
400 Gb/s	200 Gb/s	400GAUI-2 C2C C2M	400GBASE-KR2	400GBASE-CR2	400GBASE-DR2	400GBASE-DR2-2		
800 Gb/s	200 Gb/s	800GAUI-4 C2C C2M	800GBASE-KR4	800GBASE-CR4	800GBASE-DR4	1. 800GBASE-DR4-2 2. 800GBASE-FR4	800GBASE-LR4	
	800 Gb/s						TBD	TBD
1.6 Tb/s	100 Gb/s	1.6TAUI-16 C2C C2M						
	200 Gb/s	1.6TAUI-8 C2C C2M	1.6TBASE-KR8	1.6TBASE-CR8	1.6TBASE-DR8	1.6TBASE-DR8-2		

Credit: John D'Ambrosia

How Improved Media Adds Value to 200 Gbps Solutions – Electrical Links, Both Inside the Equipment and Outside



Nathan Tracy, Technologist TE Connectivity

Nathan Tracy is a Technologist on the system architecture team for TE Connectivity's Data and Devices business unit, where he is responsible for driving standards activities, providing input on new technology requirements, and working with key customers to enable new system architectures.

Nathan is active in several industry standards and associations. He currently serves the OIF as a member of the board of directors and is a regular attendee and contributor to IEEE 802.3, and Ethernet Alliance. Additionally, he is active in a number of industry MSAs and forums where he has held leadership roles.

Nathan earned his Bachelor of Science Electrical Engineering Technology degree from the University of Massachusetts, Dartmouth.



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Agenda

Enabling Architecture – what does it mean?

What's different with 200G (compared to 100G)?

Electrical Connections “Inside the Equipment”

Electrical Connections “Outside the Equipment”

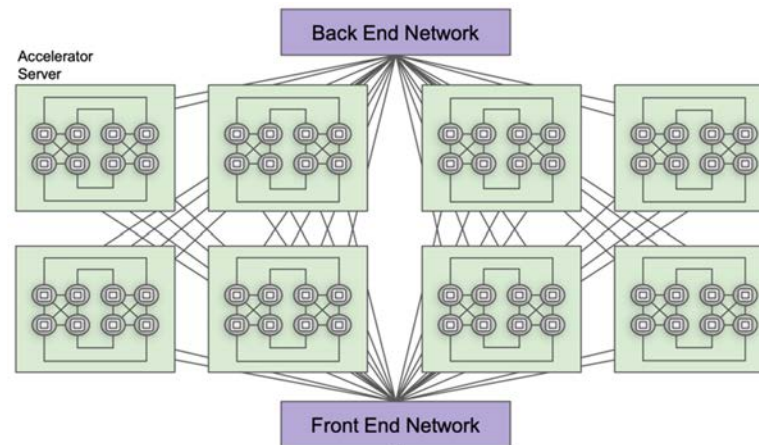
Enabling Architecture

Cloud architectures are evolving to adopt AI/ML compute technologies, driving networks to even higher levels of density. Traditional “front end” networks must increase their speed and density, while high performance or “backend” networks will require even higher densities and reduced latencies

Front end networks will continue their roadmap of doubling bandwidth every two years: 25T to 50T to 100T

Backend networks will increase node counts at lower latencies by leveraging creative architectures such as chassis systems or cabled rack concepts

Conclusion: Equipment cannot get smaller to accommodate the shorter reaches caused by higher losses at 200 Gbps signaling



Fixed Switch 100 Gbps, 64 ports @ 800 Gbps = 50 Tbps

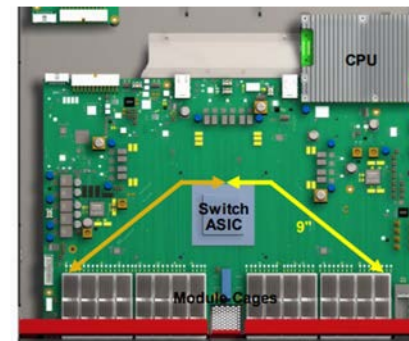


Fixed Switch 200 Gbps, 64 ports @ 1.6 Tbps = 100 Tbps

Modular Switch Faceplate: 200 Gbps, 32 ports @ 1.6 Tbps = 50 Tbps



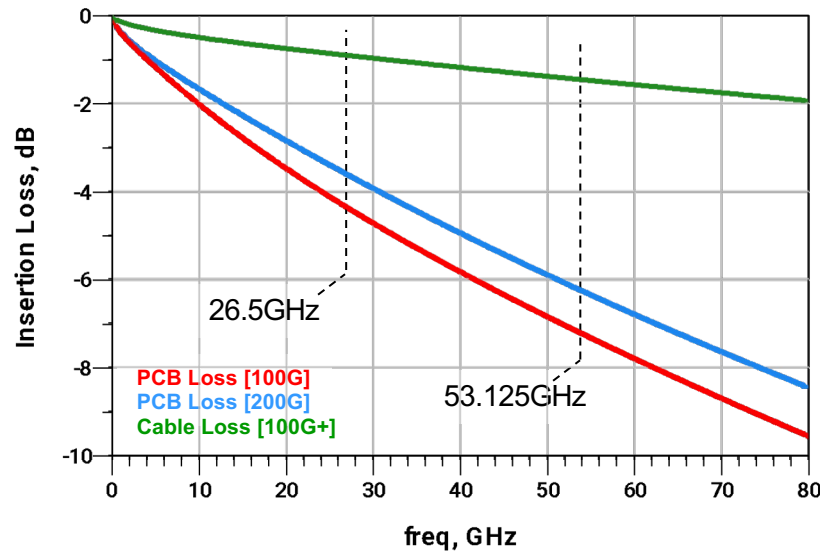
Modular Switch Backplane: 200 Gbps, 50 Tbps



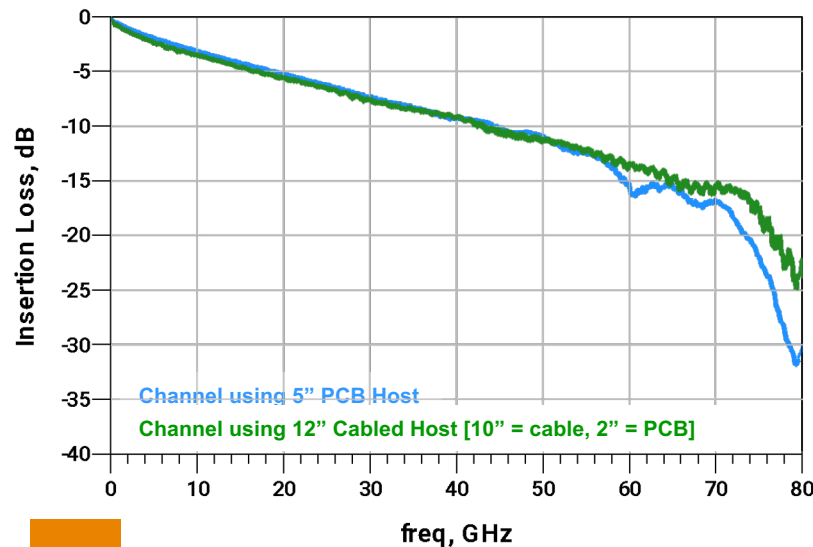
Top-down view of switch showing trace lengths required

Enabling Architecture - Continued

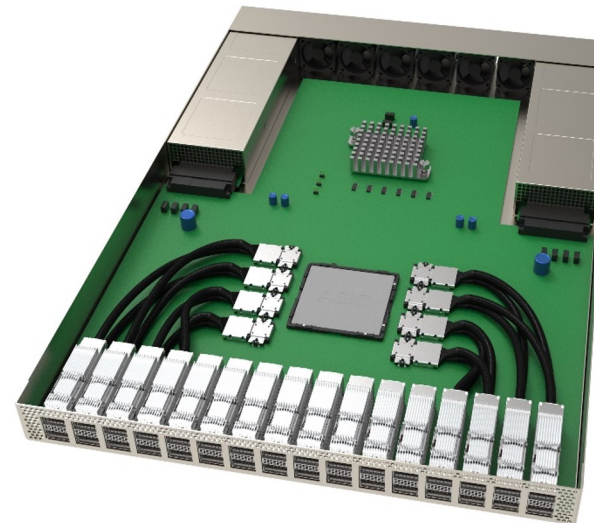
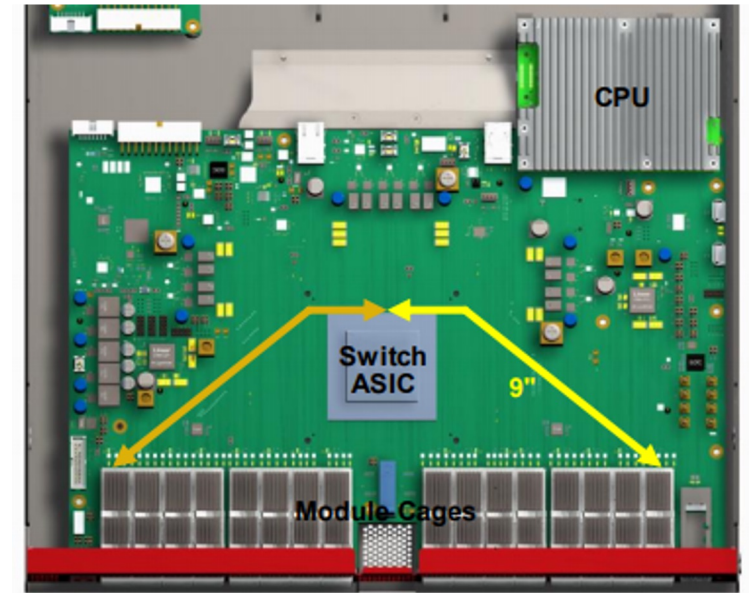
Loss Per Unit Length
Length = 5in



PCB vs. Cabled Reach, Chip to Module



- Even with improved materials and PCB technologies at 200 Gbps, the PCB trace loss increases to the point that not all signaling can reach the IO or backplane ports
- Discrete retimer chips add excessive power consumption

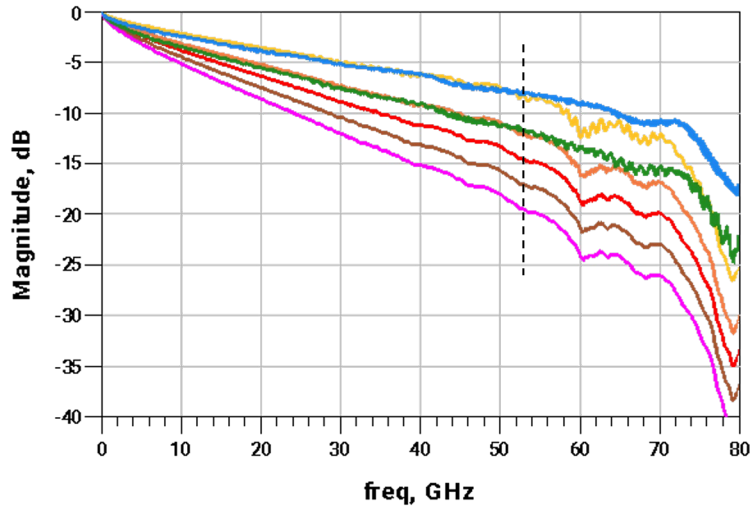


- Cabled IO ports and cabled backplane connectors will enable meeting SerDes loss budgets
- We call this OTB, i.e. Over The Board

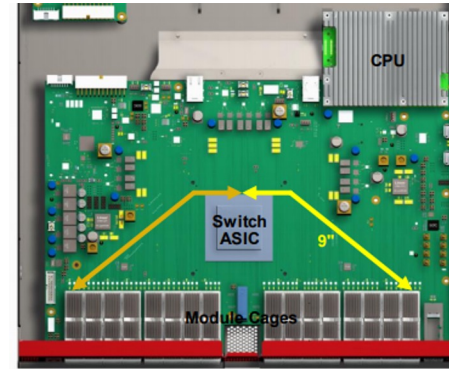
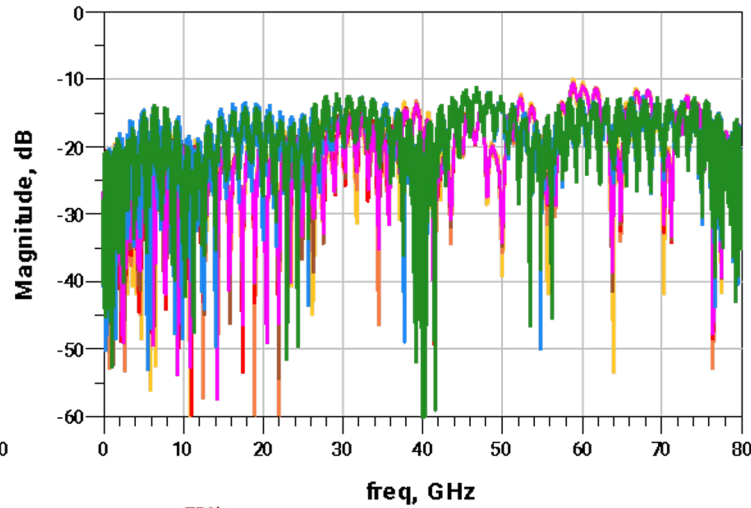
Inside the Equipment - Electrical Connections

Chip to Module (C2M) TP0 to TP1a (ball to ball) Channel Analysis

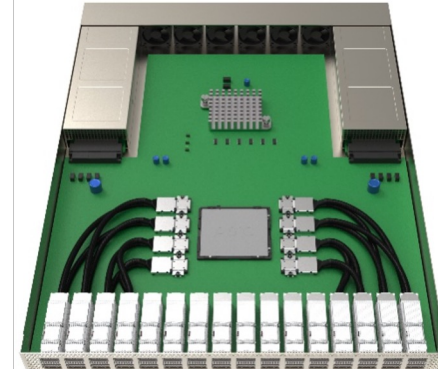
Insertion Loss



Return Loss, Module Side

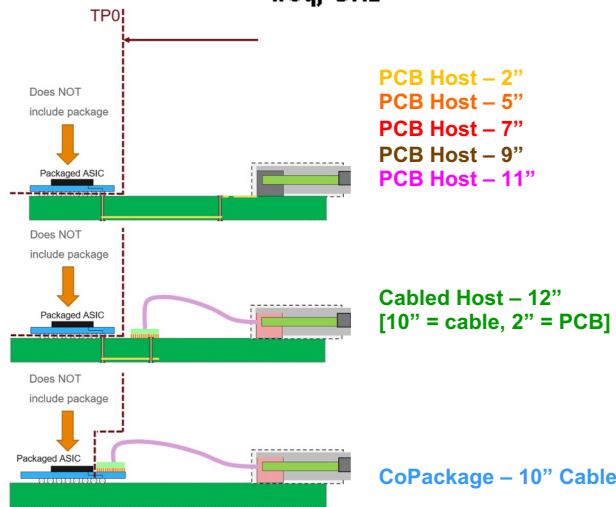
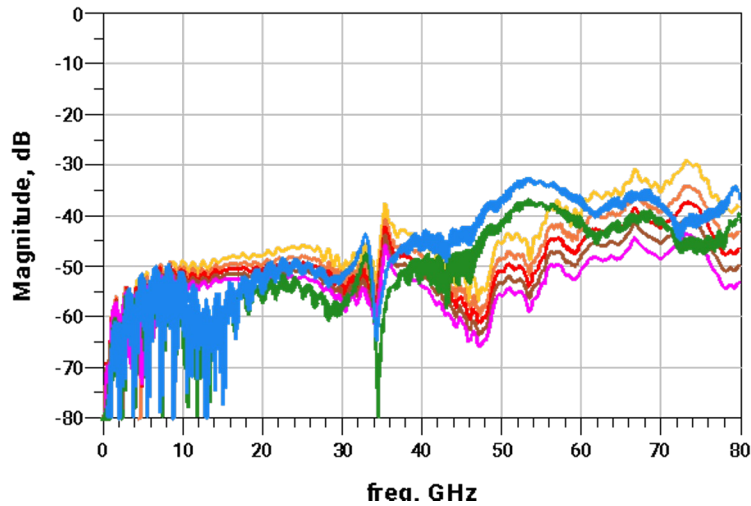


Conventional PCB traces



Hybrid design: OTB cables and PCB traces

PowerSum Cross talk, 2FEXT

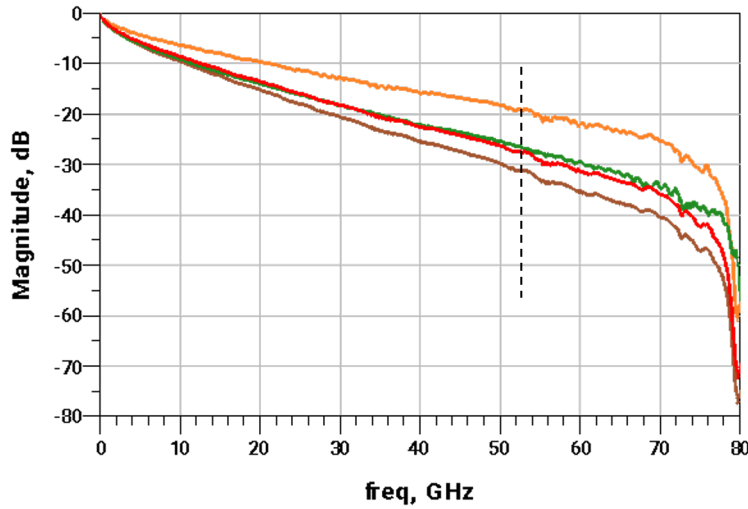


DesignCon Demo: 212 Gbps 0.5 meter OTB Cable

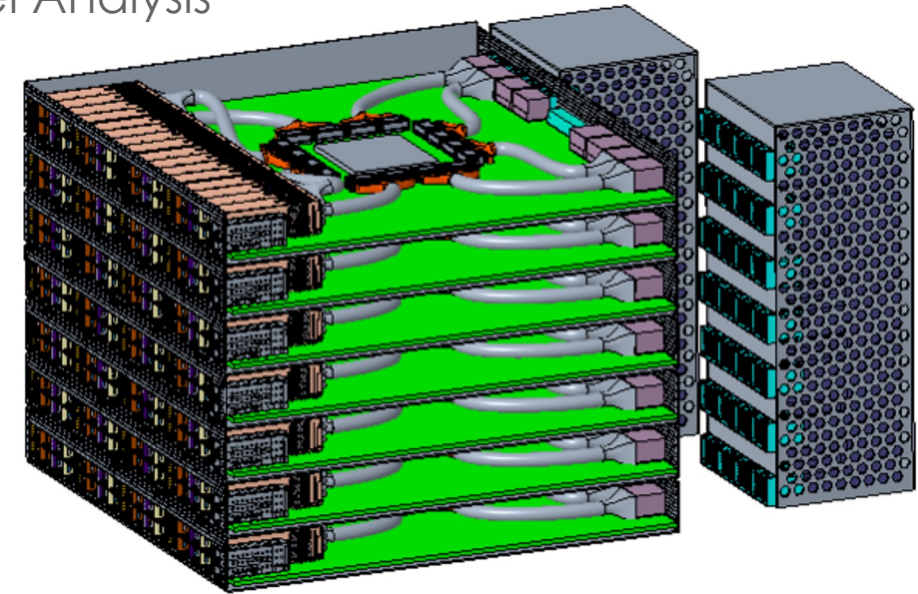
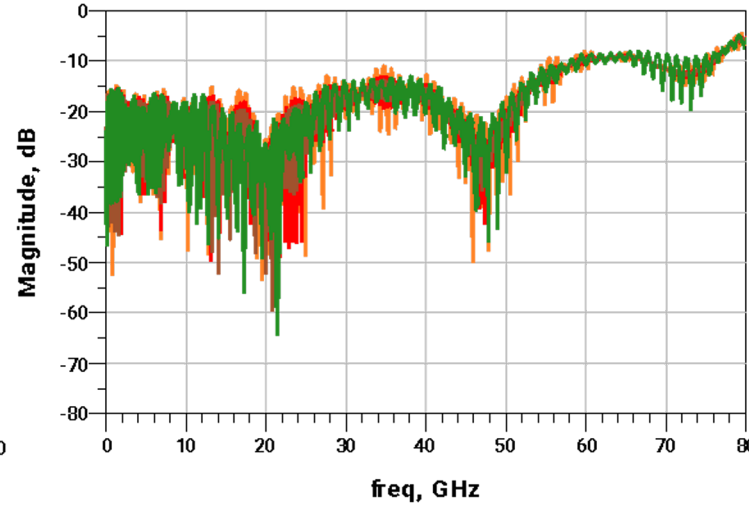
Inside the Equipment - Electrical Channels for Backplane

Line Card to Line Card Backplane TP0 to TP5 (ball to ball) Channel Analysis

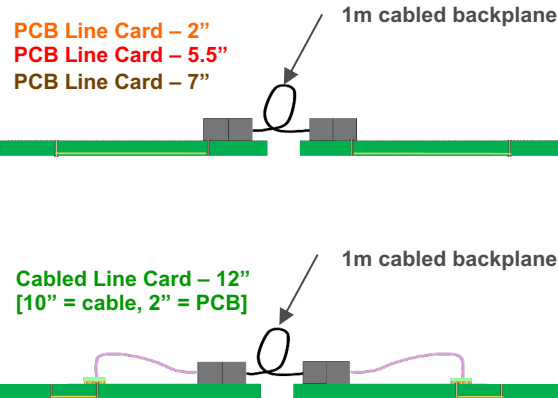
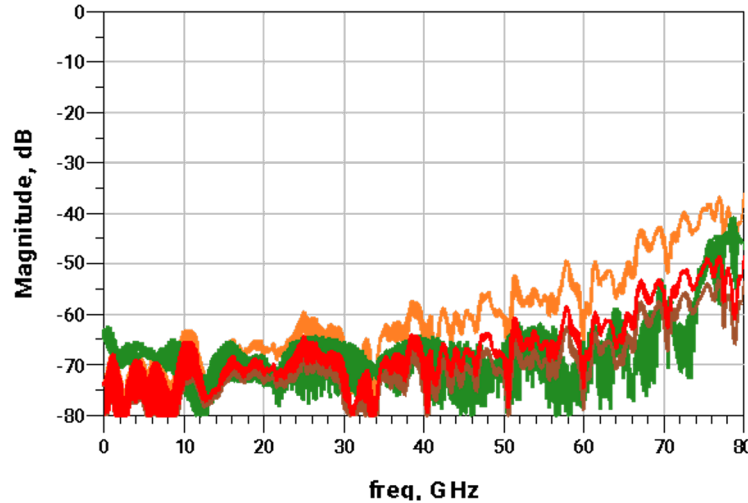
Insertion Loss



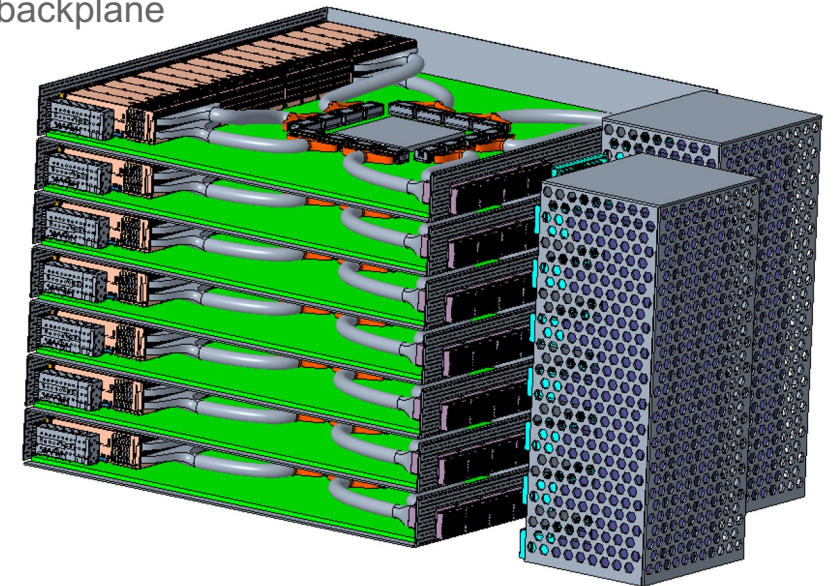
Return Loss



PowerSum Cross talk, 3 FEXT, 1 NEXT



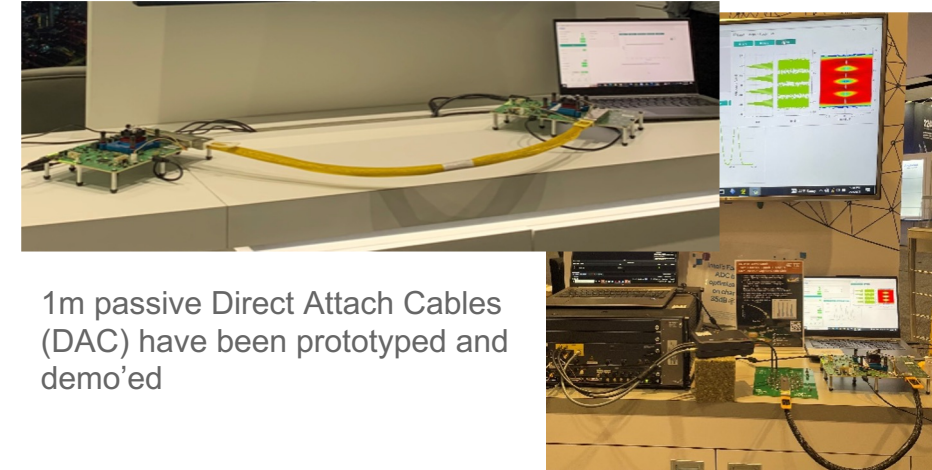
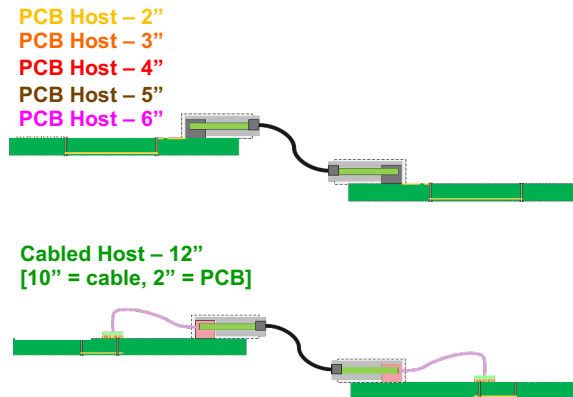
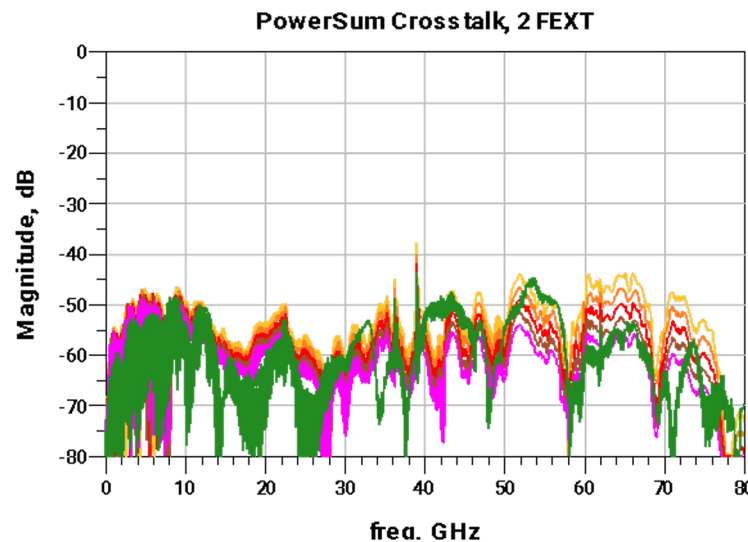
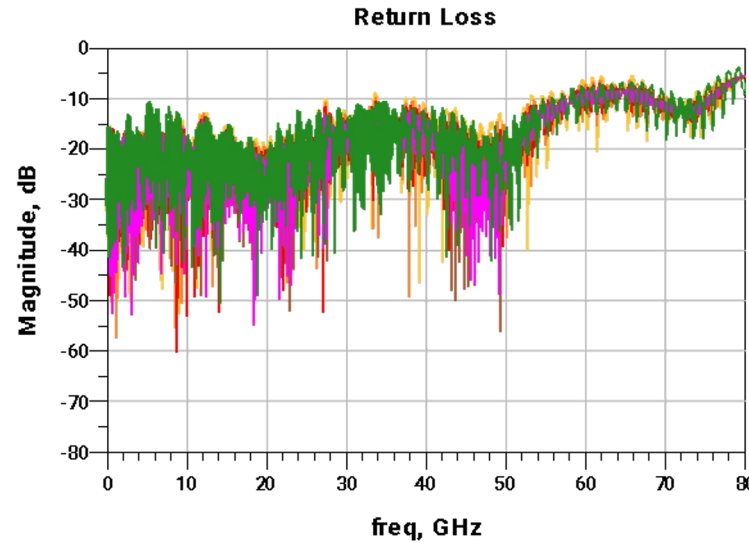
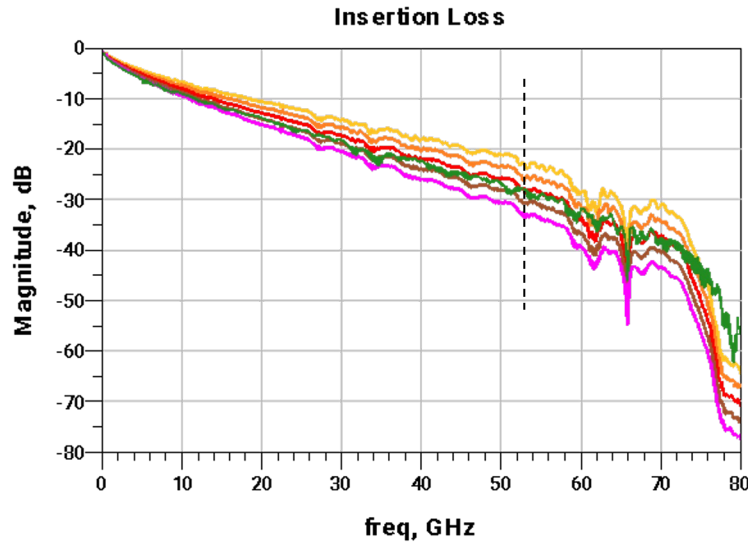
50 Terabits IO and 50 Terabits backplane



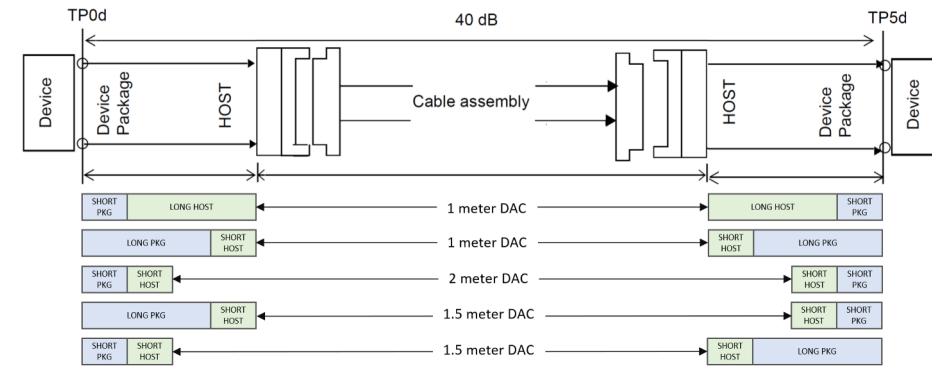
Outside the Equipment - Electrical Connections for Copper Cables



Switch to Switch (CR) TP0 to TP5 (ball to ball) Channel Analysis



1m passive Direct Attach Cables (DAC) have been prototyped and demo'ed



Asymmetrical concepts being discussed for standardization to enable longer cables

- Conventional PCB host traces and OTB cabled host implementations support 1m cables
- Active copper cables provide longer reaches than passive cables at lower cost and power than optical cables
- Both retimed cables (AEC) and non-retimed options are anticipated

Summary

IEEE P802.3dj is busy crafting solutions for the next generation data rates

At 200 Gbps, the electrical challenges are bigger than ever, but channels have been submitted and are being analyzed

There is high confidence that electrical solutions have been identified that will enable equipment architectures to continue to meet industry demands and roadmaps (satisfying reach and density)

Copper cable media, along with improved printed circuit board material and enhanced electrical interconnects is a key element to enabling these architectures

200 Gbps electrical links are challenging, requiring careful partitioning and coordination of assumptions

Optical Channels to Support 800G & 1.6T

**Gary Bernstein, Sr. Director of Global Data Center Sales
The Siemon Company**



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Nomenclature By Rate and Medium Type

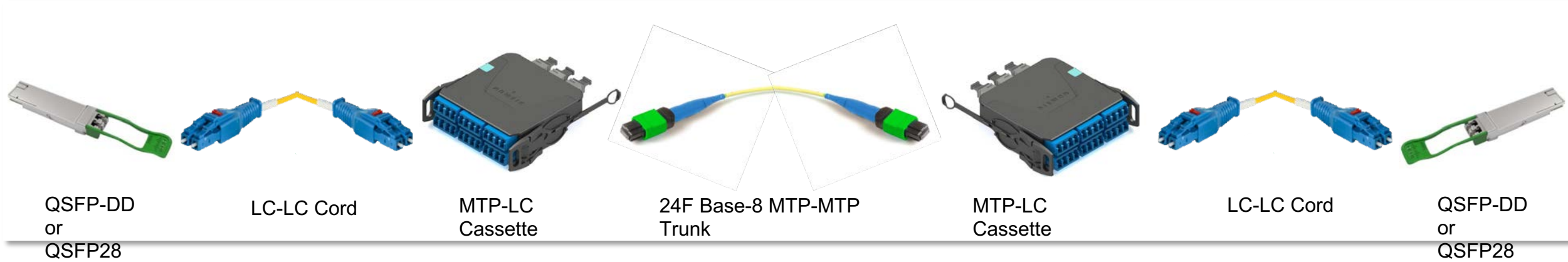
Optical PHY Options

Ethernet Rate	Assumed Signaling Rate	AUI	Backplane	Cu Cable	SMF 500m	SMF 2km	SMF 10km	SMF 40km
200 Gb/s	200 Gb/s	200GAUI-1 C2C C2M	200GBASE-KR1	200GBASE-CR1	200GBASE-DR1	200GBASE-FR1		
400 Gb/s	200 Gb/s	400GAUI-2 C2C C2M	400GBASE-KR2	400GBASE-CR2	400GBASE-DR2	400GBASE-DR2-2		
800 Gb/s	200 Gb/s	800GAUI-4 C2C C2M	800GBASE-KR4	800GBASE-CR4	800GBASE-DR4	1. 800GBASE-DR4-2 2. 800GBASE-FR4	800GBASE-LR4	
	800 Gb/s						TBD	TBD
1.6 Tb/s	100 Gb/s	1.6TAUI-16 C2C C2M						
	200 Gb/s	1.6TAUI-8 C2C C2M	1.6TBASE-KR8	1.6TBASE-CR8	1.6TBASE-DR8	1.6TBASE-DR8-2		

Credit: John D'Ambrosia

Switch to Switch: 100GDR or 400GFR4 Channel

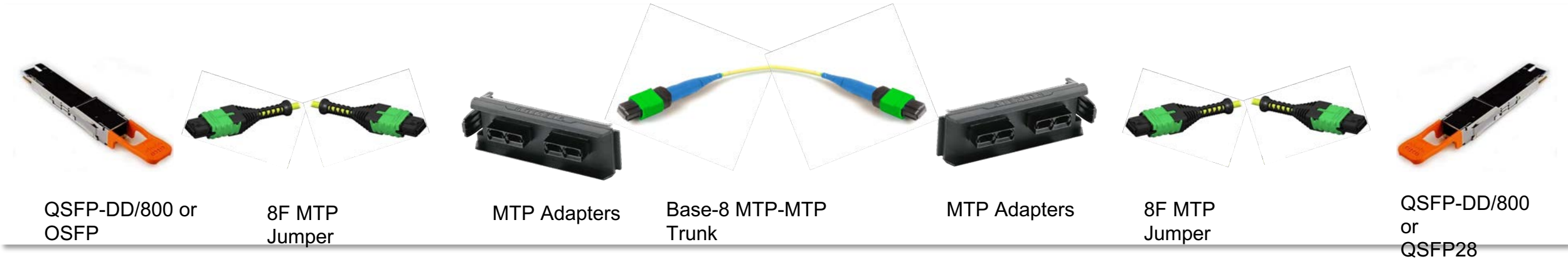
2-fiber Singlemode Channel will support 10G, 40G, 100G & 400G



- Base-8 Singlemode cabling
- Provides duplex LC connections at equipment

Switch to Switch: 100G PSM4, 400G DR4 or 800G DR4 Channel

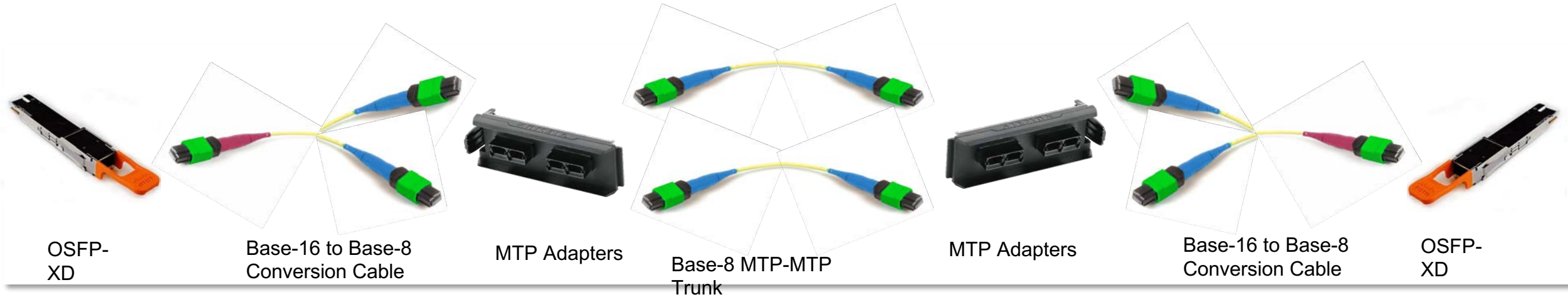
8-fiber Singlemode Channel will support 40G, 100G, 400G & 800G



- Base-8 Singlemode cabling
- Provides parallel (8-fiber) connections at equipment

Switch to Switch: 1.6T-DR8 Channel

Base-8 Singlemode Channel with conversion to MPO16 connection at switch



- Base-8 Singlemode cabling
- Provides parallel (16-fiber) connections at equipment

DSP Technologies for 200G



Tony Chan Carusone, Chief Technology Officer Alphawave Semi

Dr. Tony Chan Carusone has taught and researched integrated circuits and systems for high-speed connectivity in industry and academia for over 20 years. He has been the Chief Technology Officer of Alphawave Semi since 2022 and a faculty member at the University of Toronto since completing his Ph.D. there in 2002. He has received eleven best-paper awards at leading conferences for work on chip-to-chip and optical communication circuits, analog-to-digital conversion, and precise clock generation. He also co-authored the latest editions of the classic textbooks "Analog Integrated Circuit Design" and "Microelectronic Circuits," the best-selling engineering textbook of all time. He is a Fellow of the IEEE.

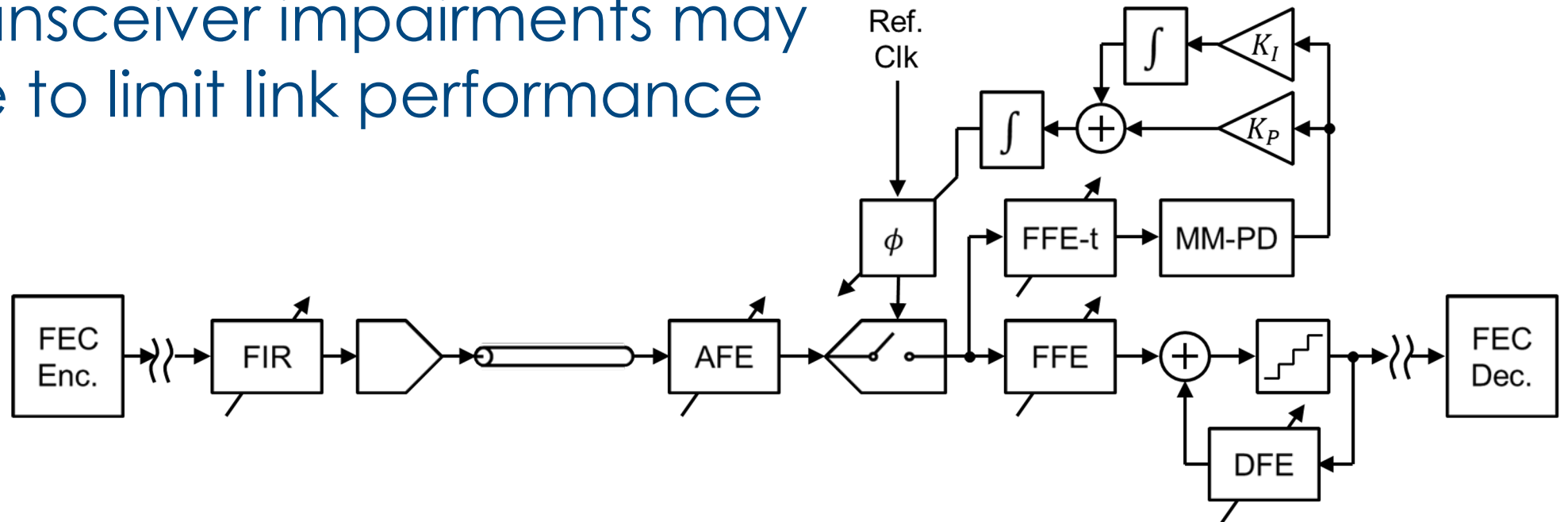


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Impact of Transceiver Impairments

- Many transceiver impairments may combine to limit link performance at 200G:

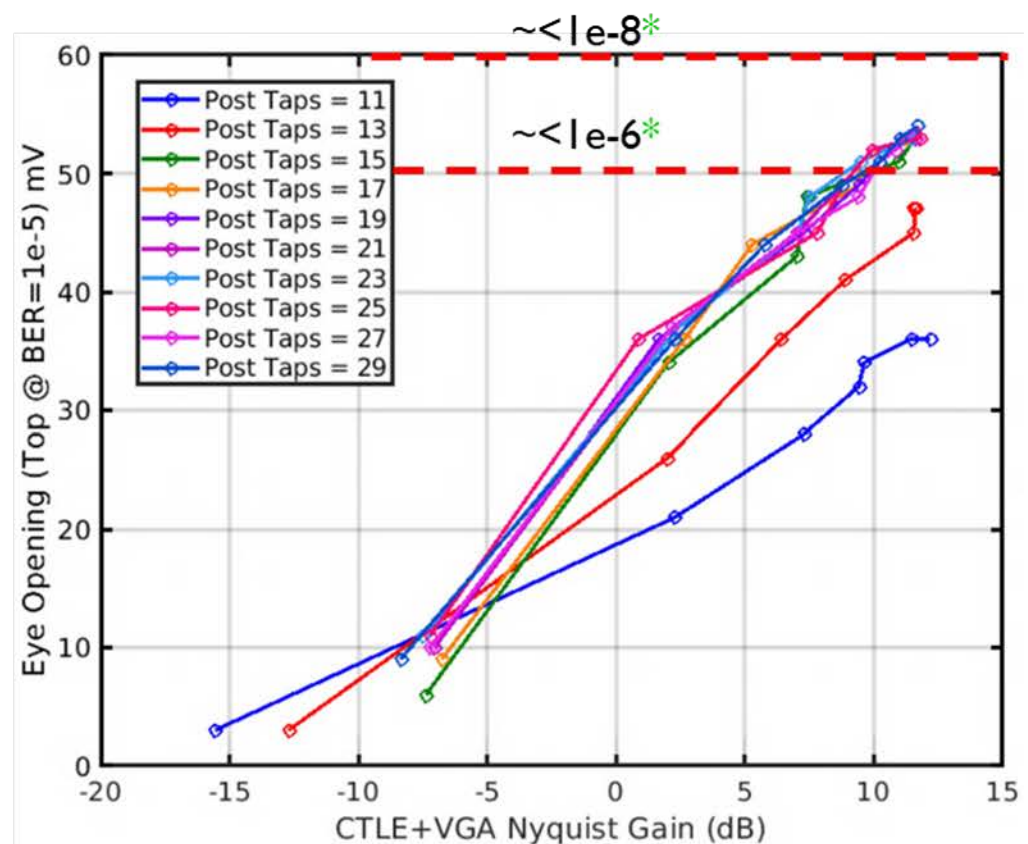
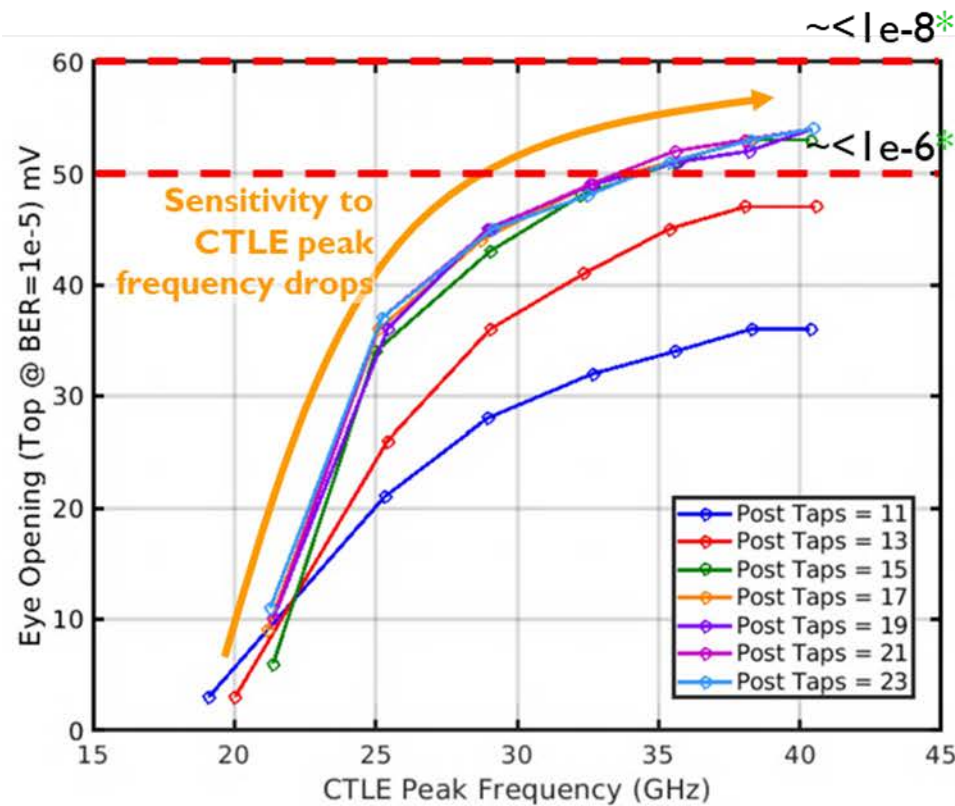


- Analog front-end noise, distortion, ADC imperfections, ...
- ISI (insufficient equalization)
- Sampling clock jitter



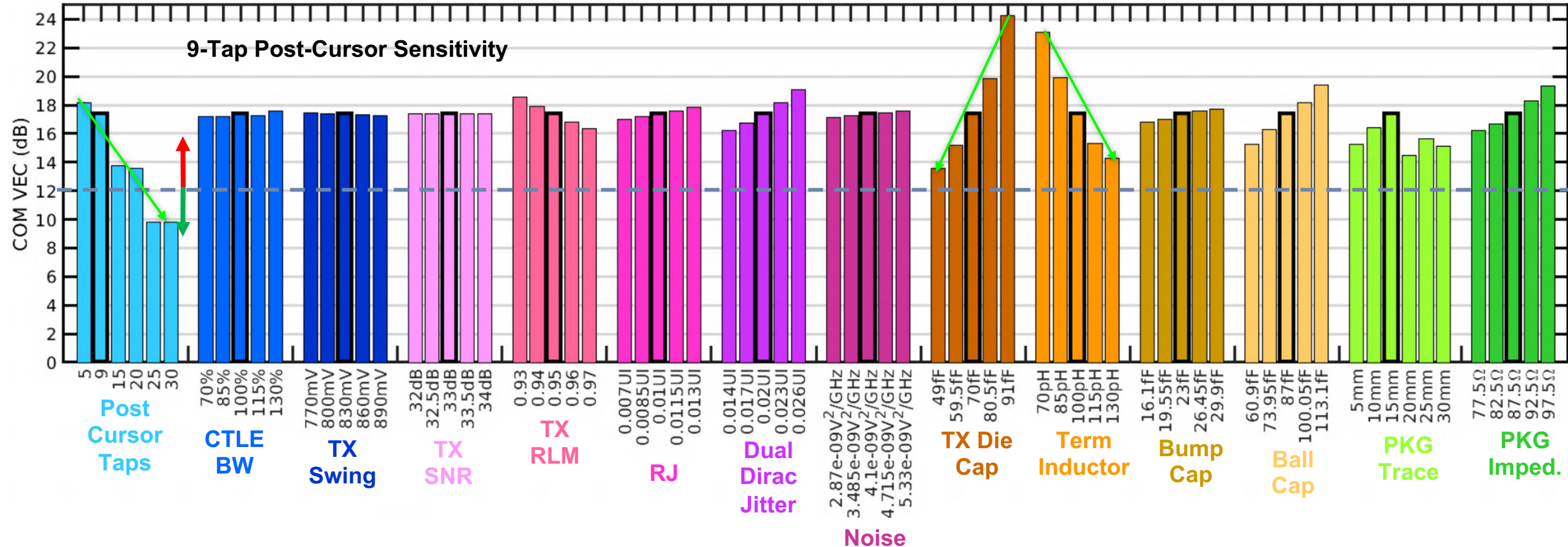
DSP Directly Mitigating Analog Limitations

Impact of FFE tap count on CTLE requirements for Chip to Module Channel



System Impairment Sensitivity

At 200G, links can be extremely sensitive to termination and package discontinuities unless highly capable equalizers are provided

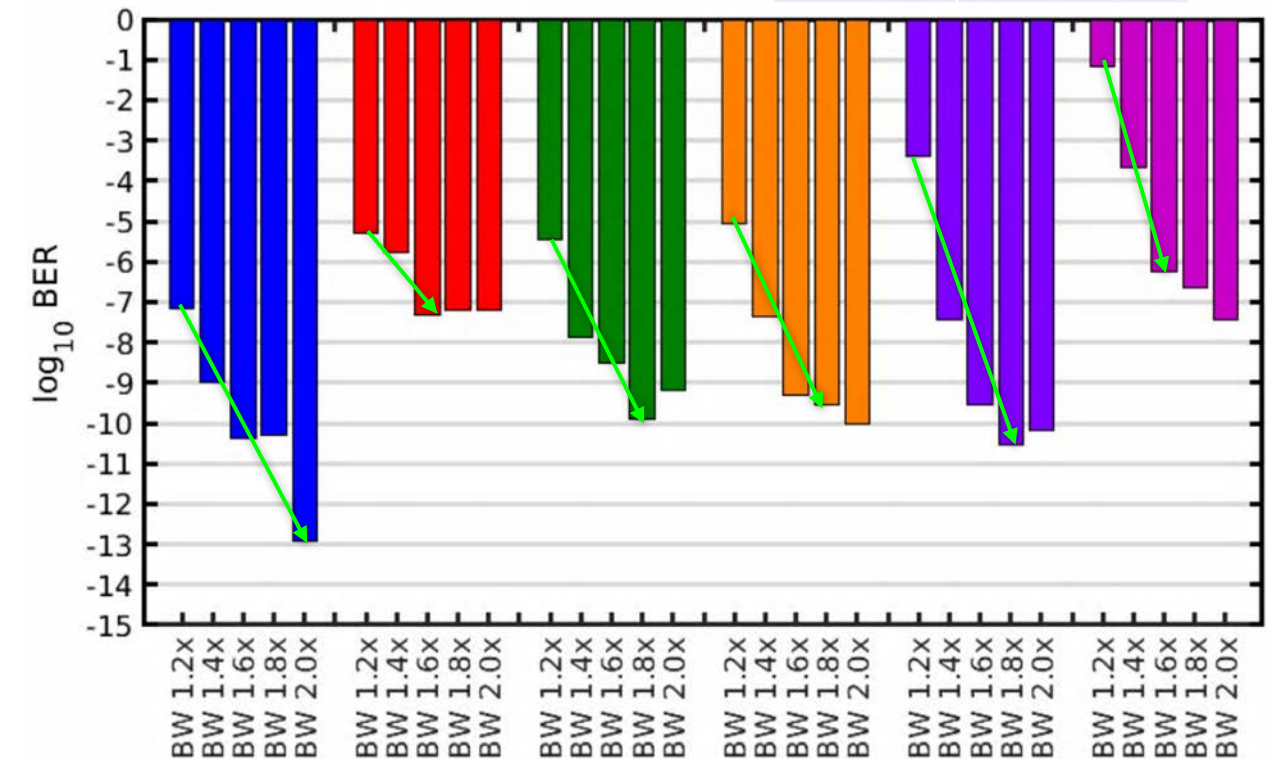
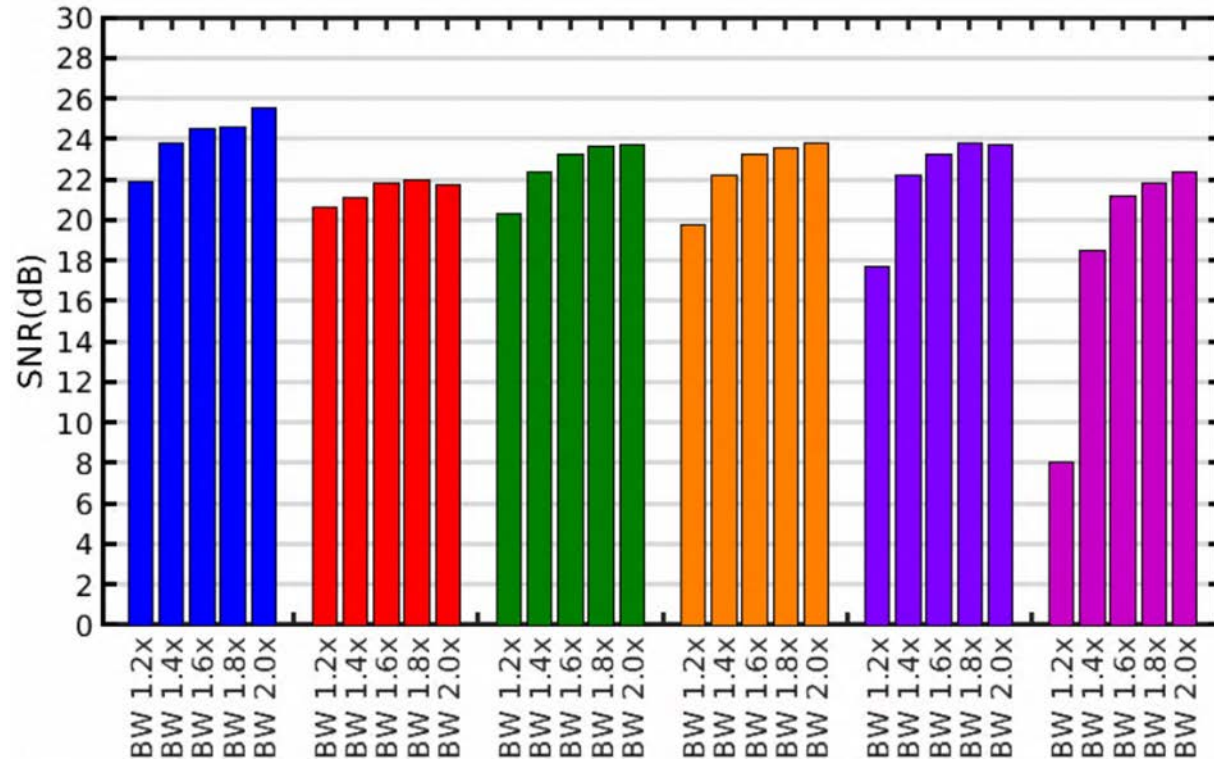


200G Bandwidth Requirements

With extensive DSP (35 Tap FFE + 1 Tap DFE), target BER can be met by scaling bandwidth only 1.6x compared to a 100G transceiver

□ Even in Channels 5 & 6 having > 30dB loss

Channel Number	Loss @ 53.125GHz
1	-7.4 dB
2	-12 dB
3	-18 dB
4	-28.1 dB
5	-33.4 dB
6	-38.6 dB



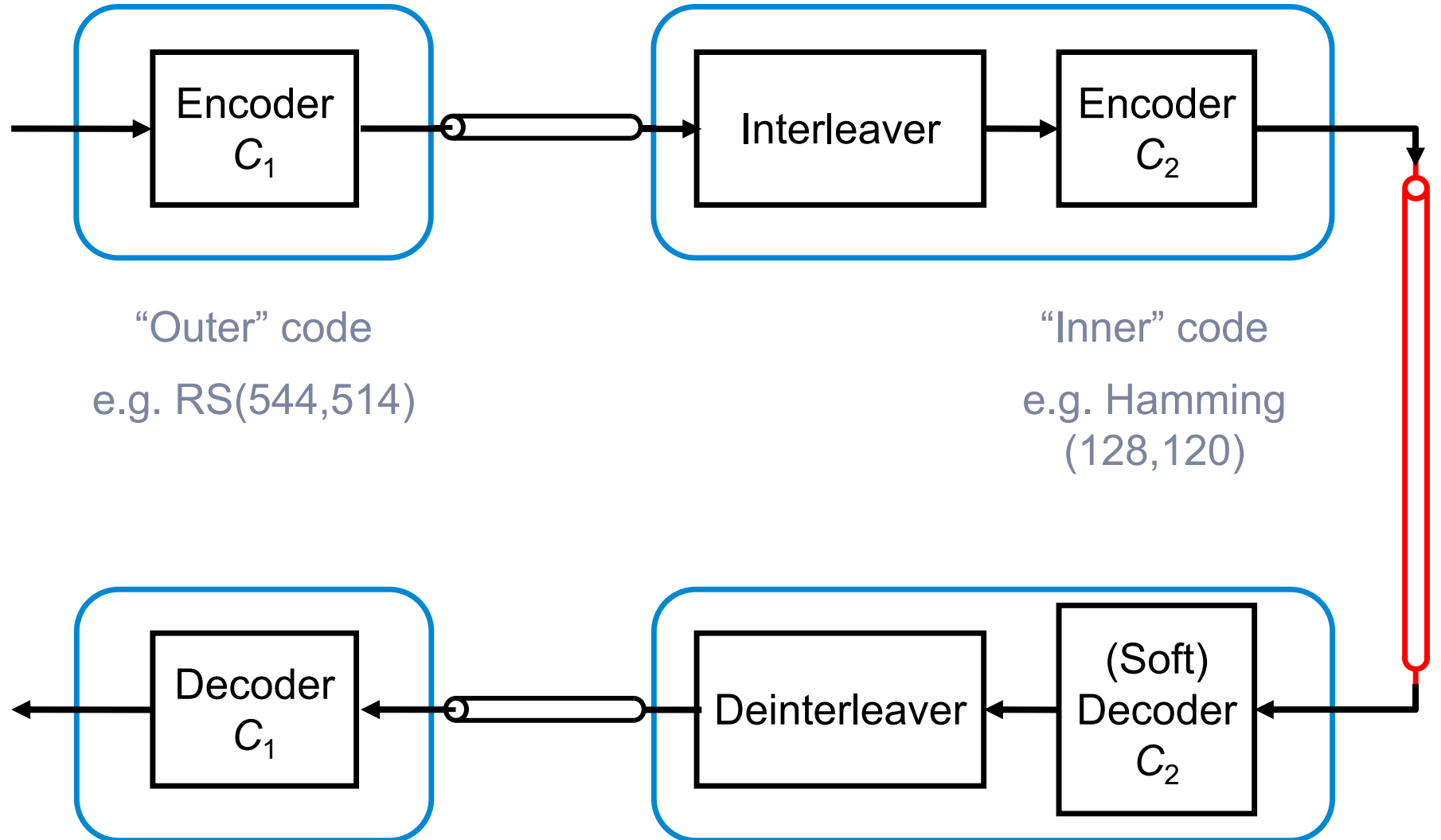
Channel: 1 2 3 4 5 6

Channel: 1 2 3 4 5 6



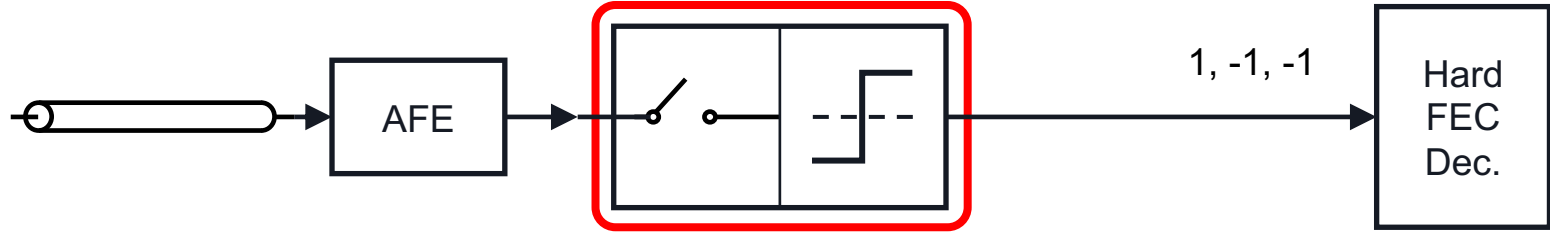
Concatenated FEC at 200G

- Coding gain is improved by concatenating codes
- Burst-error correction performance is a key consideration
⇒ aided by an interleaver
- Encoding/decoding functions and coding gain may be spread across multiple hops
- Trade-offs to be evaluated: higher baud rate, higher latency, higher power consumption

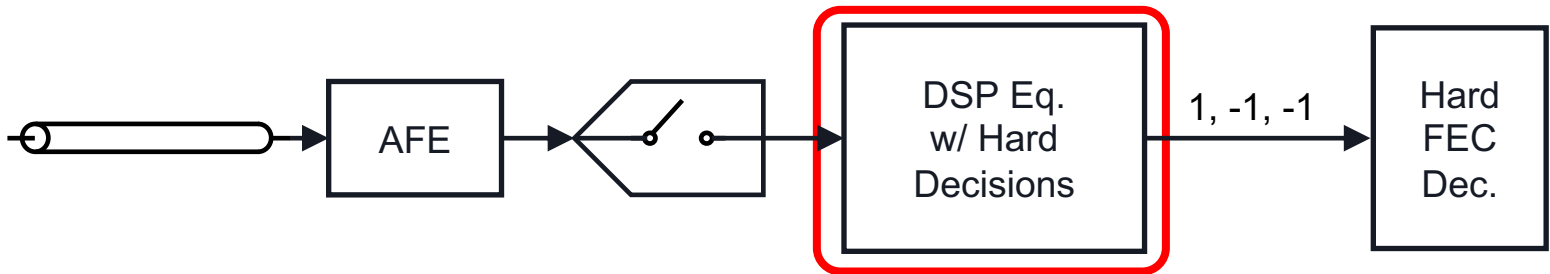


Architectural Impact of Soft FEC

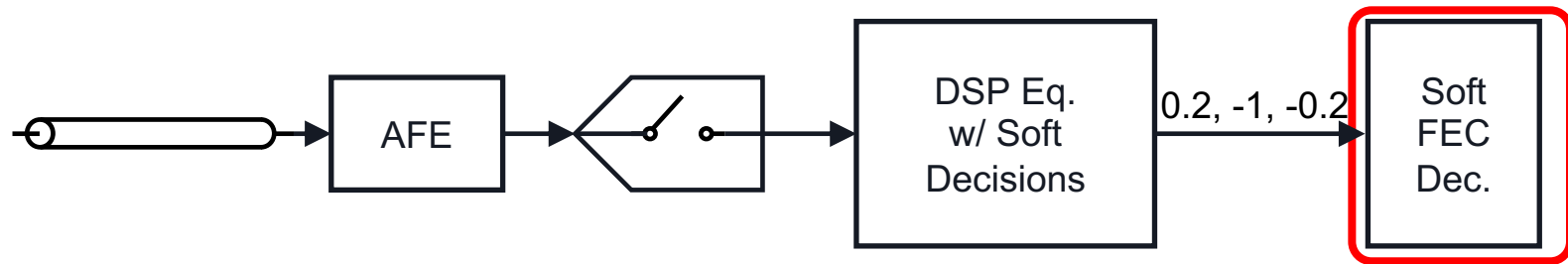
- **Strong potential for soft decision FEC technology to be used at 200G**
- Effectively precludes traditional analog SERDES architectures
- Require substantially tighter integration between the FEC and AFE



Analog SERDES \Rightarrow Hard decisions made along with analog sampling



ADC Based DSP SERDES \Rightarrow Hard decisions made in the DSP



ADC Based DSP SERDES \Rightarrow Digitized decision made in the FEC



Summary



Many transceiver impairments combine to limit link performance at 200G



New DSP technologies: Extensive equalization, MLSD, C-FEC & S-FEC



Tradeoffs between link margin, latency, DSP power consumption, optics power consumption, etc.



Shrinking design margins necessitating tighter co-optimization of all aspects of the link



212G Physical Layer Overview



**John Calvin, Strategic product planner for high performance networking technology
Keysight**

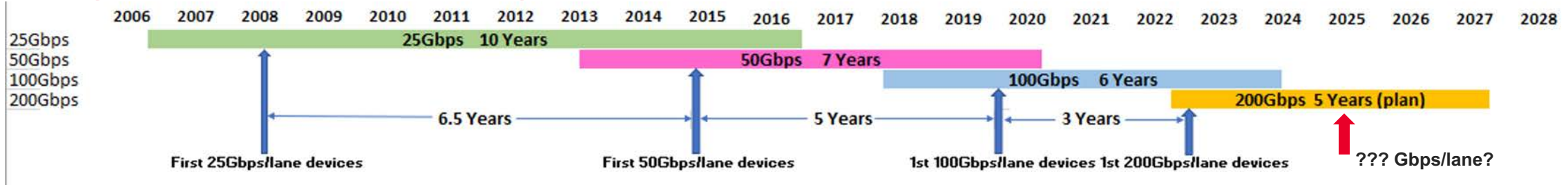
John Calvin is a strategic planner and DataCom technology lead for Keysight Technologies. John has been bridging the measurement science gaps of emerging Telecom and DataCom development efforts for 20 years. He serves on the Ethernet Alliance board of directors and is a contributing senior member to IEEE 802.3, OIF-CEI, InfiniBand, and PCIe development efforts. John holds a BSEE from Washington State University, and his graduate level studies are in signal processing from Stanford University.



ethernet alliance

www.ethernetalliance.org

High Speed Networking Standards Compression



The drive to power reduction on a “pico-Joule per bit” basis, is key to Hyperscaled Data Center architecture and scalability objectives.

- Process geometry reductions 5nm 3nm 1.8nm all points of discussion now. Halving the geometry ~ translates to $\sim\sqrt{2}$ power reduction.
- Increases in signaling rates “sending double the bits in half the time interval” require more complex signal compensation methods which draw more power and present complex benefit tradeoffs.
- Higher order modulation methods offer better spectral utilization, but latency tends to track upwards too.

The Hyperscalers DC Equipment CAPEX has grown to \$150B/yr ^{R1} (+17%) in 2023

- 102.4Tb/s Switch RFQ’s are currently in circulation today with aggressive competition
- OFC 2023 saw the rapid expansion of 212G capable Phy’s with 6 distinct solutions emerging

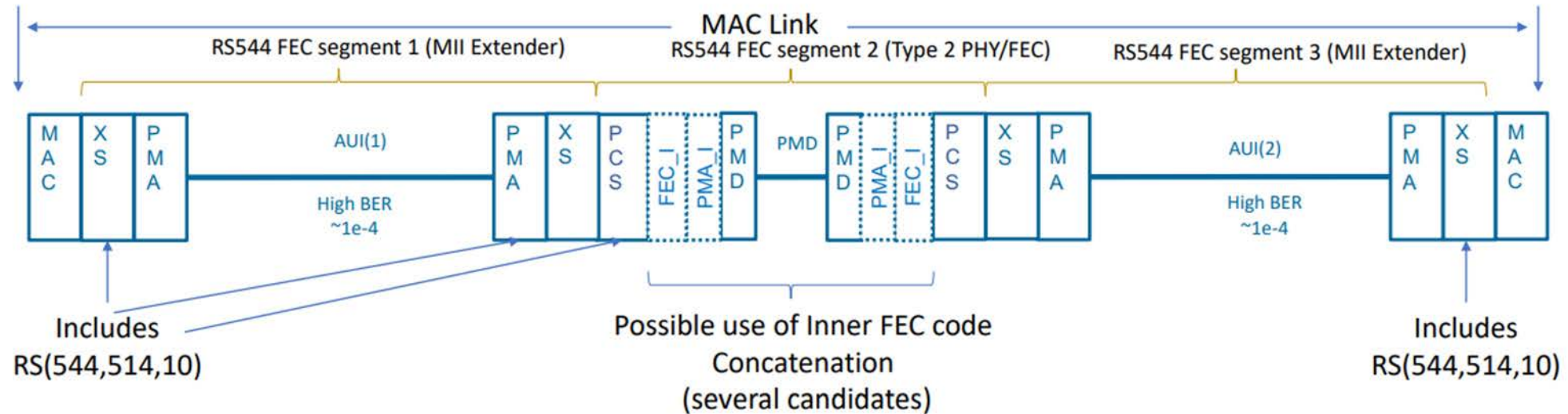
The cycle of technology rollout is compressing by ~15% per iteration.

R1 Source:360 Group: (DC_Total_Market_and_Forecast_Report Table 5)

IEEE Recent Developments (As of March Plenary Atlanta)

(IEEE reference: https://www.ieee802.org/3/dj/public/23_03/gustlin_3dj_01_2303.pdf)

- Type 2 (High BER AUI's illustrated here) have been incorporated into .3dj with the use of an inner 128/120 (Hamming) Concatenated FEC which increases the inner link speed to 113



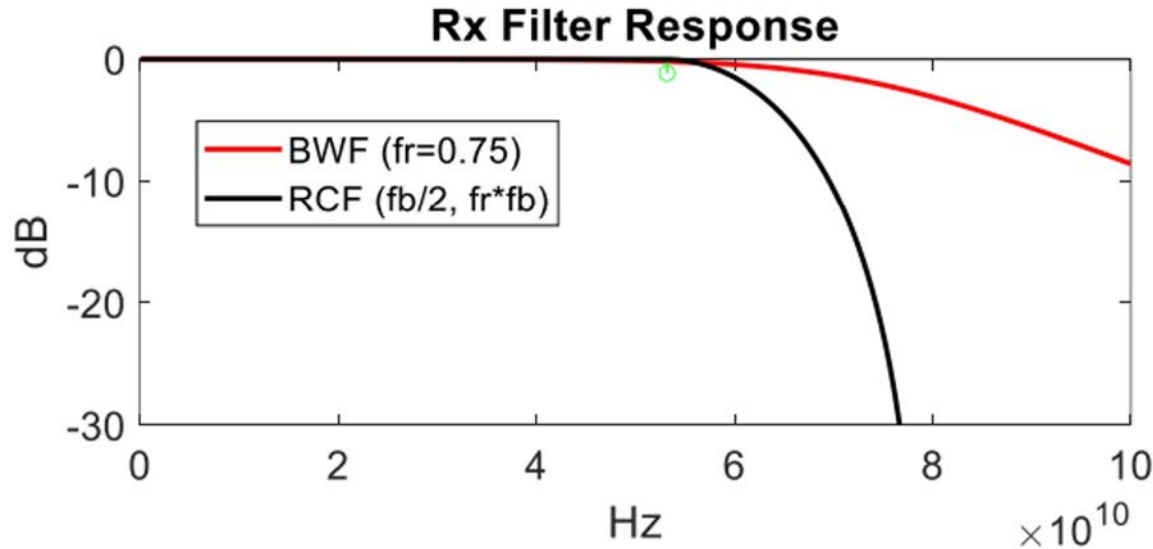
- Type 2 PHY/FEC with no AUIs on either side
- MII Extender on both sides with one high-BER AUI each
- Current assumption: High BER AUIs targeting $\sim 1e-4$ require XS
 - Isolates errors from the high BER AUI
 - PMD can't take advantage of this, must support worst case
 - Two extenders in this example
- Input BER to PMD portion of the link ~ 0
- Highest latency option due to XS across the AUI(1) and AUI(2) (does not consider FEC inner code decision)

Proposed 212Gbps Reference Receiver Bandwidth

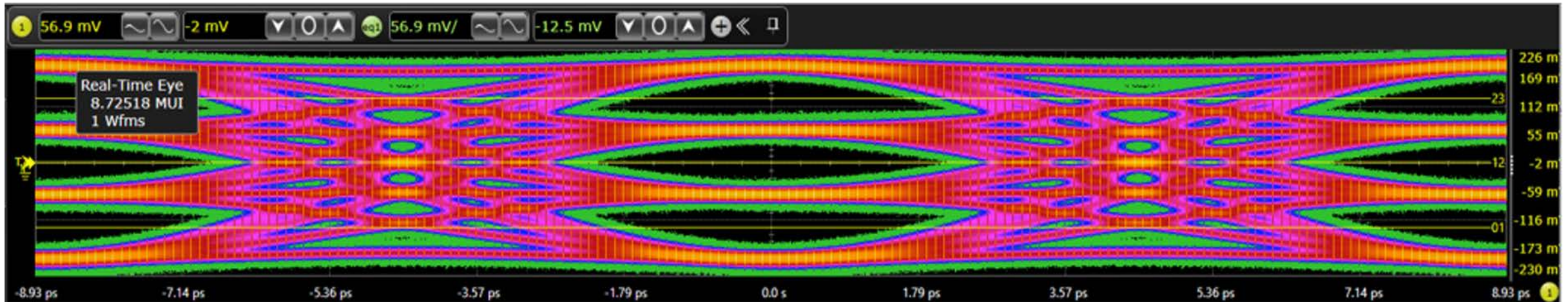
IEEE Reference: https://www.ieee802.org/3/df/public/adhoc/electrical/22_0621/mellitz_3df_elec_01b_220621.pdf

-or- OIF Reference (oif2022.462.0/Pg 12): <https://www.oiforum.com/bin/c5i?mid=4&rid=7&gid=0&k1=53279>

High loss package compensation and Reference Receiver for 212-224 Gbps

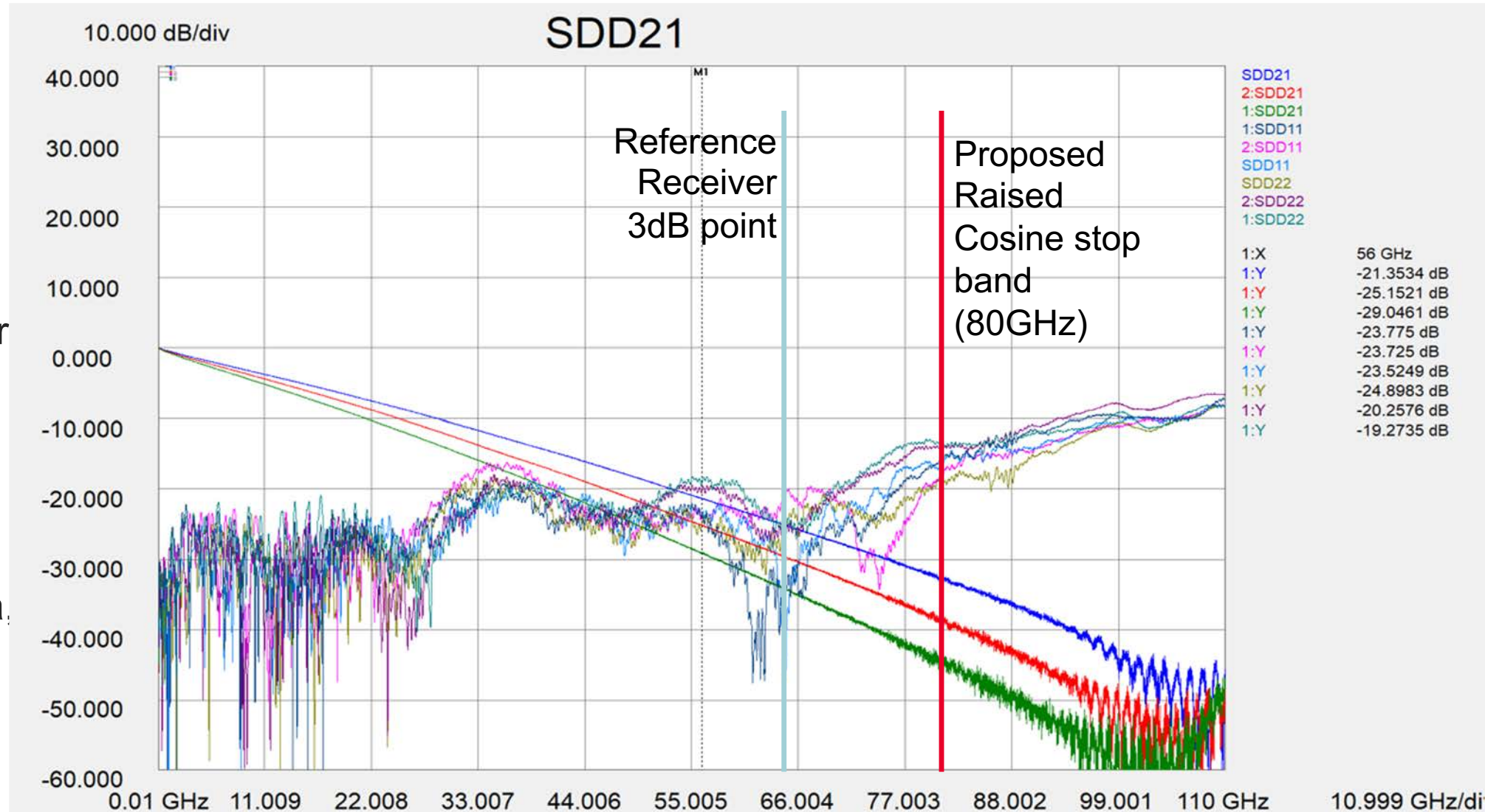


Both IEEE 802.3df and OIF-CEI 224G have reviewed, reference receiver channel proposals based on a combination of Raised-Cosine and Butterworth filters which balance noise (BUN) rejection along with near Nyquist Bandwidth specifications. It's been demonstrated empirically and with COM simulations that 212Gbps Reference Receiver optimum performance is a balancing act between Nyquist and NEXT/FEXT BUN contributions.



Frequency Dependent Attenuation

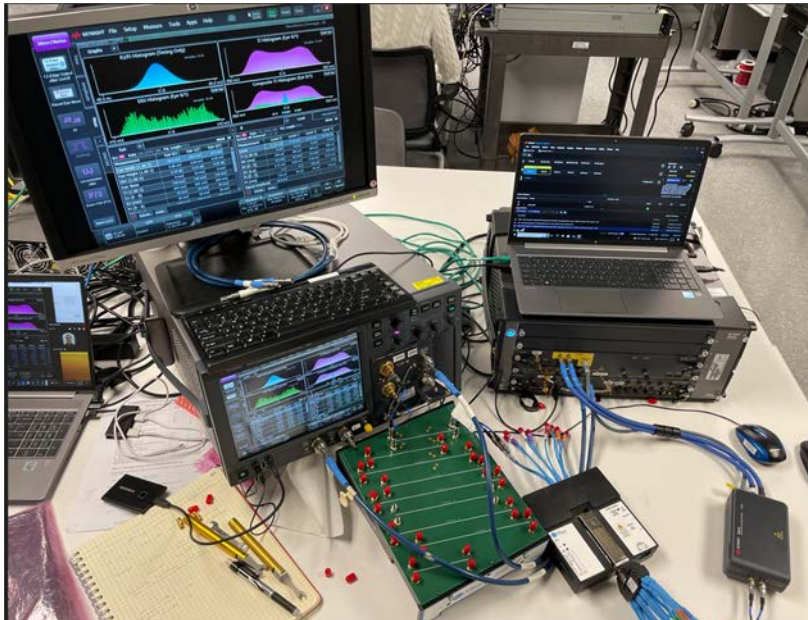
- An example FDA, showing resonance free operation into the proposed Reference Receiver bandwidth areas.
- Reflections well below -15dB
- Specifications are still fluid in this area, but this is an example of what's possible today.



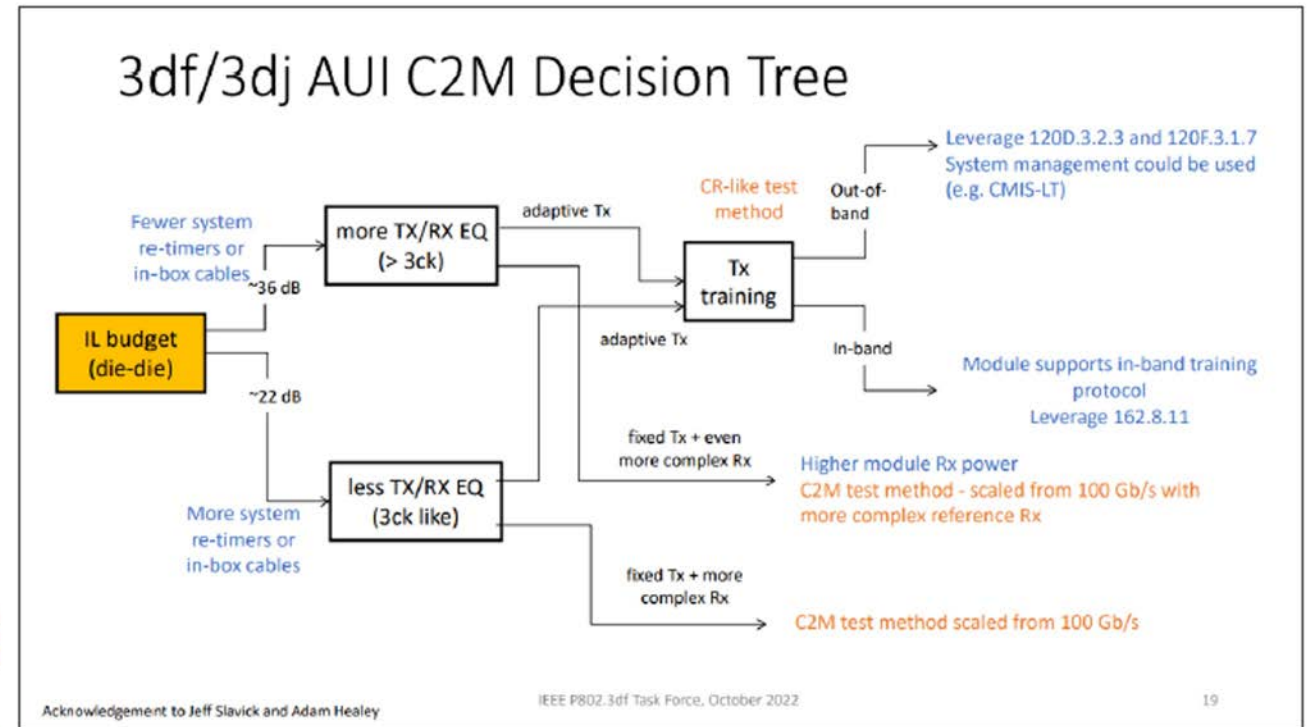
Source: Wilder Technologies

212G Science Projects related to AUI loss considerations

Source: [lusted_3df_01_220927 : https://www.ieee802.org/3/df/public/22_10/22_0927/lusted_3df_01_220927.pdf](https://www.ieee802.org/3/df/public/22_10/22_0927/lusted_3df_01_220927.pdf)



AUI interaction with optical PMDs development



The likelihood of a TP0d->TP1a or TP2 loss profile ranging from 22-36dB is a very real prospect in 212G architectures.

Performing a traditional signal characterization after 34dB of loss is a very significant complication and a challenge for existing measurement techniques.

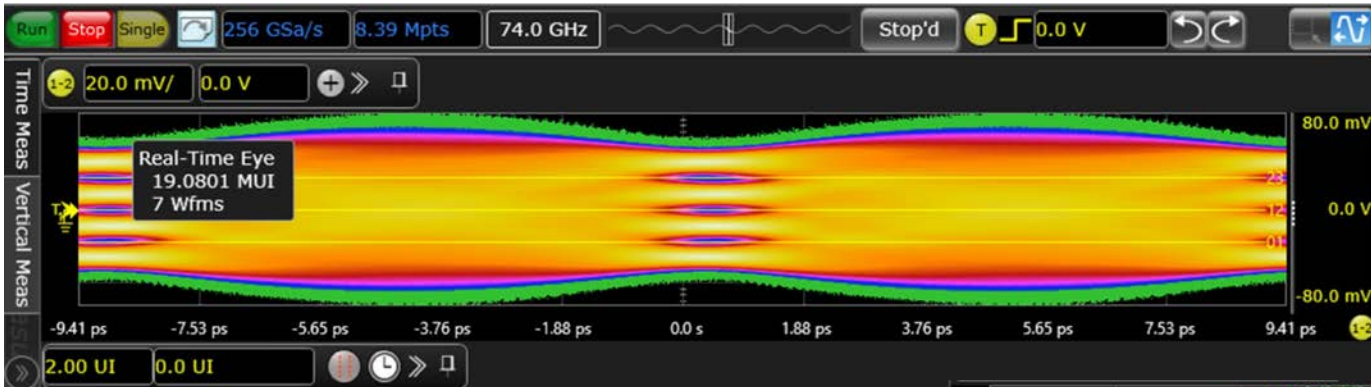
Ref TX & RX

SerDes/AUI DER	1e-5	5e-5	1e-4
802.3ck C2M like	19.97	21.44	22.27
802.3ck C2M like + FLT	21.37	22.88	23.67
802.3ck CR like	31.75	33.5	34.37
802.3ck CR like + MLSE	36.5	38.13	38.82

Source: [li_3dj_02a_2303.pdf : https://www.ieee802.org/3/dj/public/23_03/li_3dj_02a_2303.pdf](https://www.ieee802.org/3/dj/public/23_03/li_3dj_02a_2303.pdf)

212.5Gbps through a MTF + Host FDA (net 34dB loss) –w- RTO (80GHz)

A Real-Time (over-sampled) Oscilloscope is the only system which can perform required 1st order 4MHz PLL CDR tracking at 200+Gbps today. High loss conditions are a challenge but workable condition.



PAM4 Jitter

Channel 1 - 2 Various No graphs

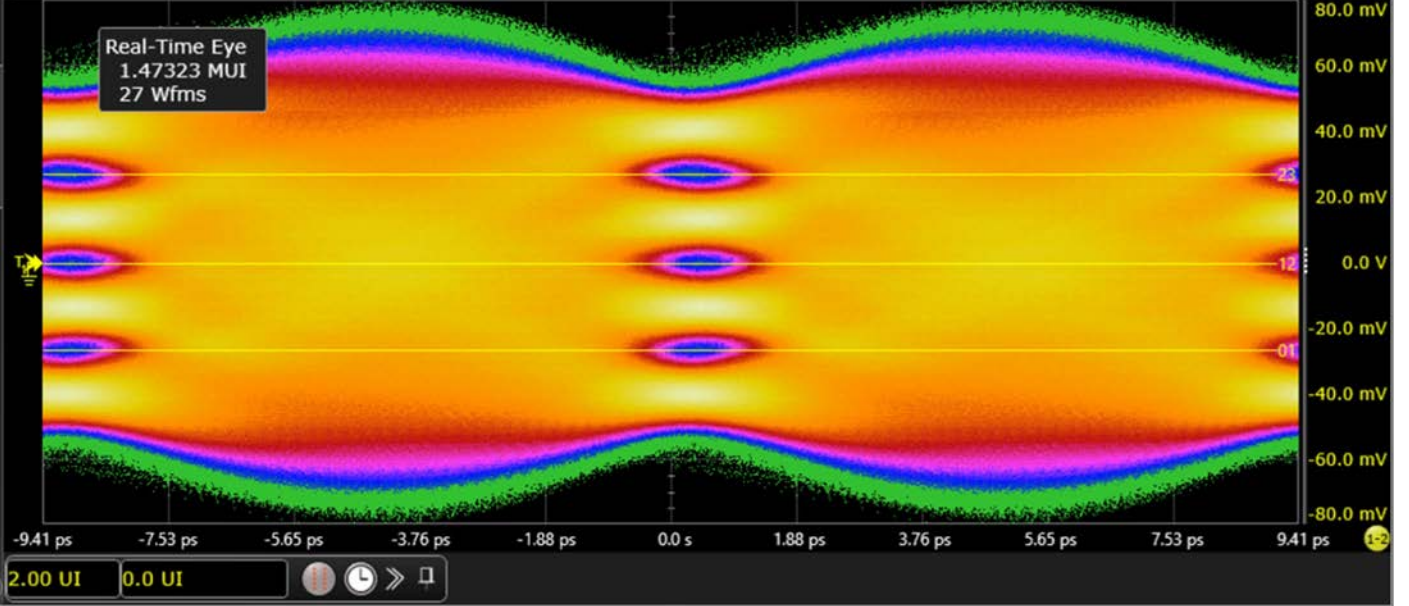
Ch 1-2 J3u Table (2884 Patterns)				Ch 1-2 Jrms Table (2884 Patterns)			
From	To L0	To L1	To L2	From	To L0	To L1	To L2
All	439.668 mUI			All	50.3692 mUI		
L3	157.038 mUI	205.280 mUI	379.820 mUI	L3	23.1423 mUI	30.8030 mUI	53.7108 mUI
L2	216.153 mUI	393.948 mUI		L2	32.6056 mUI	51.4030 mUI	
L1	356.352 mUI		584.384 mUI	L1	49.1203 mUI		71.1877 mUI
L0		462.810 mUI	188.838 mUI	L0		63.0210 mUI	28.9911 mUI

Results (Measure All Edges)

Measurement	Current	Mean	Min	Max
Eye 1/2 Height(1-2)	5.5 mV	5.5 mV	5.5 mV	5.5 mV
Eye 0/1 Height(1-2)	5.0 mV	5.2 mV	5.0 mV	5.3 mV
Eye 2/3 Height(1-2)	5.6 mV	5.9 mV	5.6 mV	5.9 mV

Color Grade

- 1 - 668
- 669 - 1337
- 1338 - 2675
- 2676 - 5351
- 5352 - 10702
- 10703 - 21405



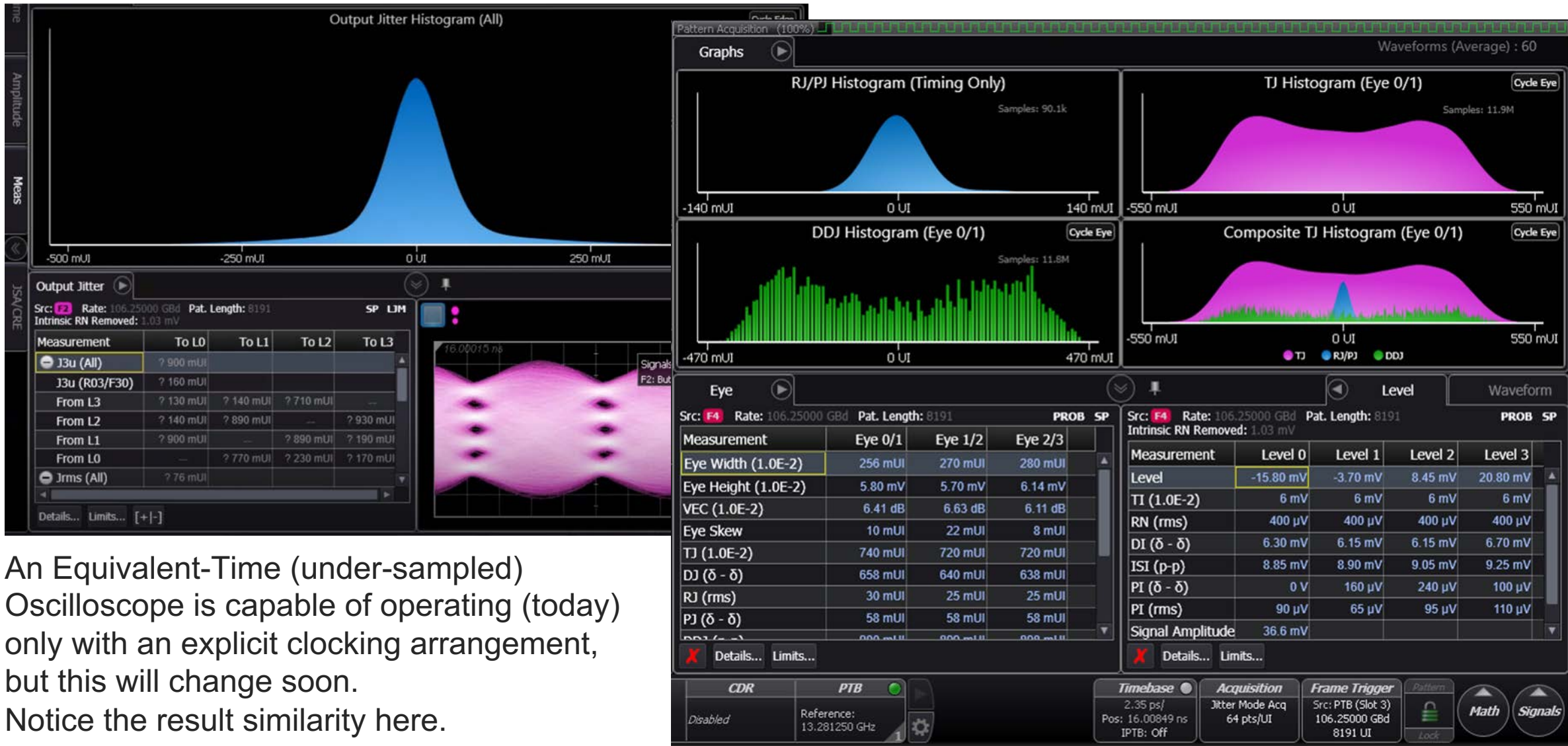
Results (Measure All Edges)

Measurement	Current	Mean	Min	Max
Eye 0/1 Height(1-2)	5.3 mV	4.53 mV	1.9 mV	5.3 mV
Eye 1/2 Height(1-2)	5.6 mV	4.84 mV	1.9 mV	5.8 mV
Eye 2/3 Height(1-2)	6.1 mV	5.41 mV	2.2 mV	6.7 mV

Color Grade

- 1 - 20
- 21 - 40
- 41 - 81
- 82 - 163

212.5Gbps through a MTF + Host FDA (net 34dB loss) –w- ETO (80GHz)



An Equivalent-Time (under-sampled) Oscilloscope is capable of operating (today) only with an explicit clocking arrangement, but this will change soon. Notice the result similarity here.

2023 212Gbps Pilot Silicon Demos

Advanced 1.6T Research

Test 224 Gb/s electrical Tx



Intel Falcon-2 EVB 224G-LR Prototype

224G-LR TEST EVALUATION SYSTEM



Intel Falcon 224Gbps 8P ADC based SerDes reformed for operation in channels of up to 20dB @ 50GHz NVQ

- 6 (5 new) 224G silicon providers demoed in 2023
- All are targeting IEEE CR/OIF LR channel loss configurations which are at the upper performance extreme of 40dB TP0d->TP5d



Thank you!

If you have any questions or comments, please email admin@ethernetalliance.org

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