

Defining 400 Gbps per Lane Electrical and Optical Signaling for Ethernet

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[Champion for [IEEE 802.3 Mar 2026 CFI - 400Gbps Signaling Ethernet Project](#)]

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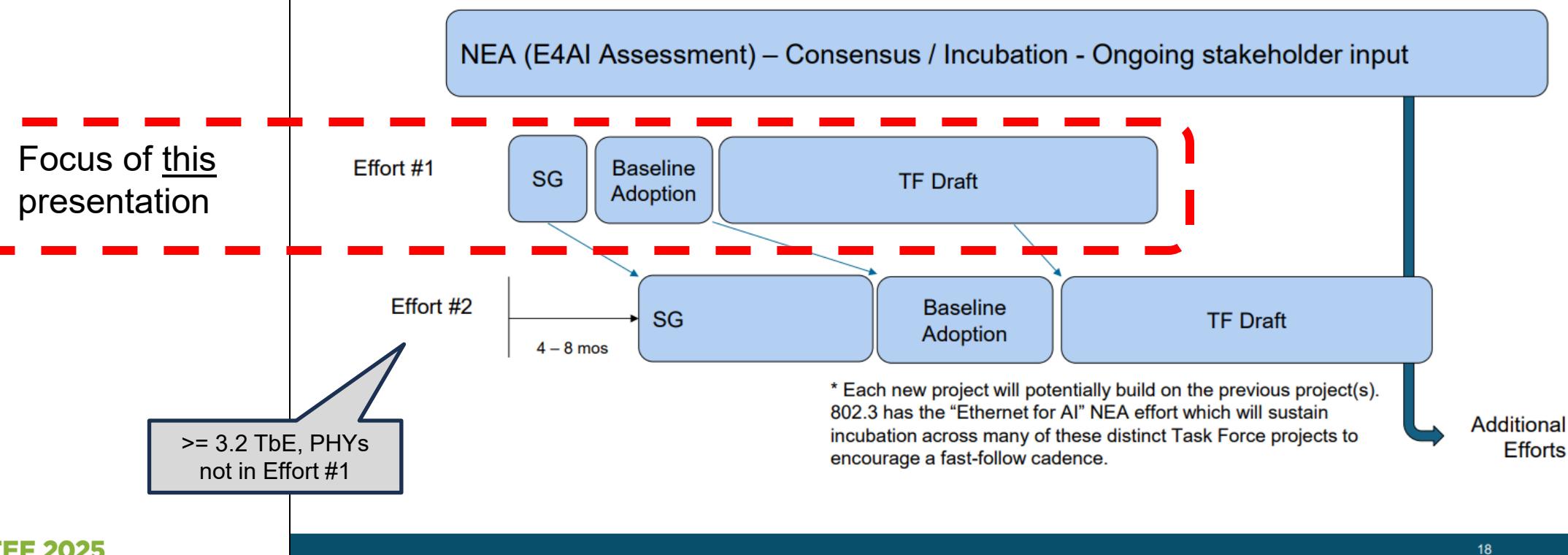
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The Effort(s) Interconnect Implications Getting Started Now

Two Efforts Forming In the Pipeline

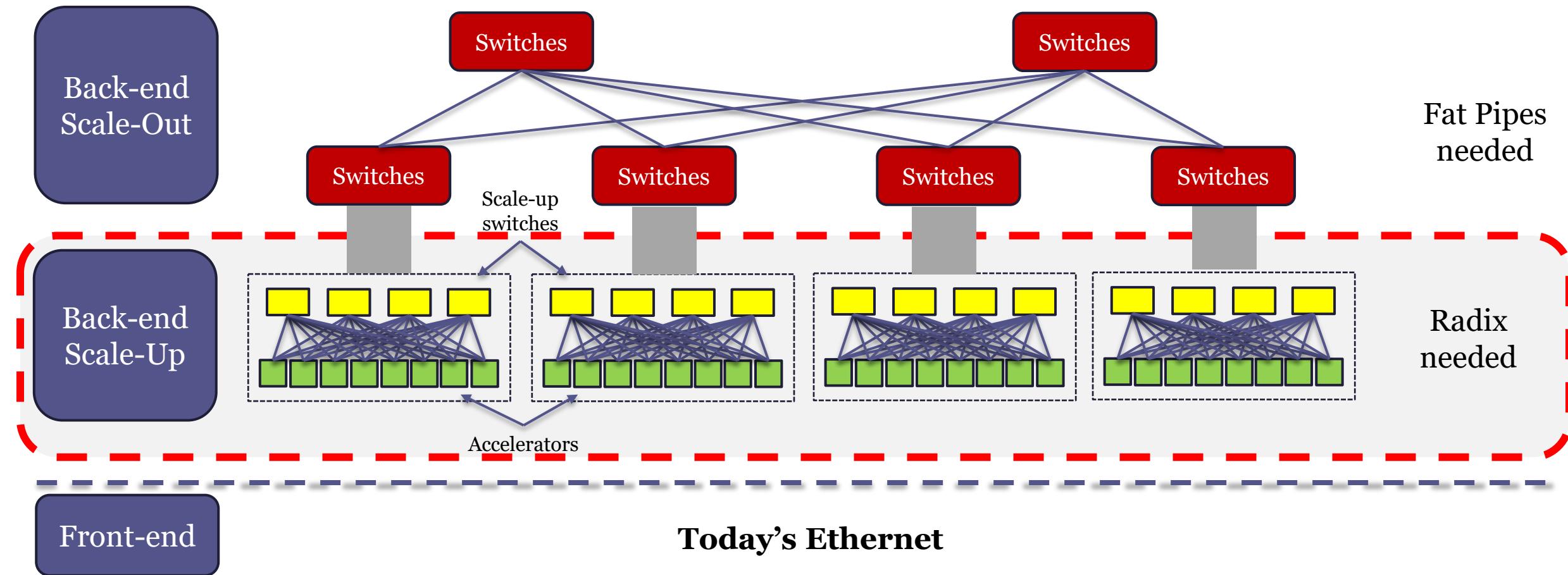
Moving Forward in IEEE 802.3



Looking Forward and Moving Fast

- AI Back-end “scale-up” networks are driving higher signaling rates first
 - Followed by scale-out
 - Then front-end networks
- Scale-up = high radix (flat network, lots of x1/x2 links)
- Copper is known for low cost & power and high reliability, but the reach is shrinking
- Optics have a growing footprint in scale-up (and scale-out)
 - Co-packed optics (CPO) are increasingly important

AI Datacenter Network Hierarchy

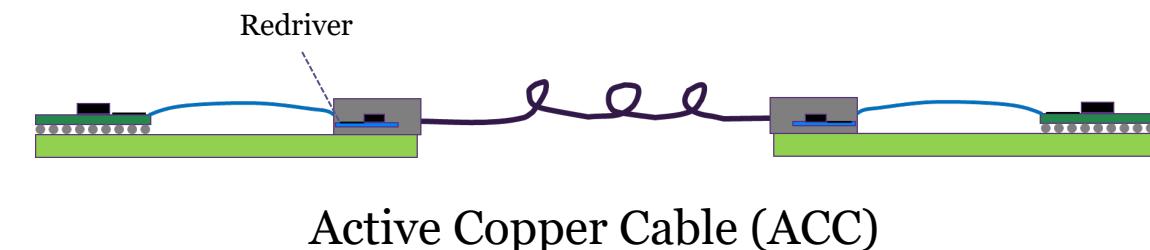
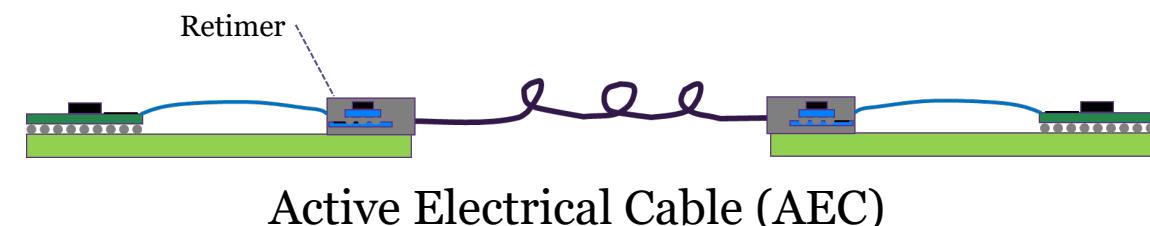


The Effort(s) Interconnect Implications Getting Started Now

Copper Interconnect at 400 Gbps/lane

- Reach limitations of passive copper emphasizes the need for active solutions
 - Passive:
 - Well known and well-established methodologies
 - AEC:
 - Comparable to a pluggable optical transceiver
 - ACC:
 - Not well specified across industry

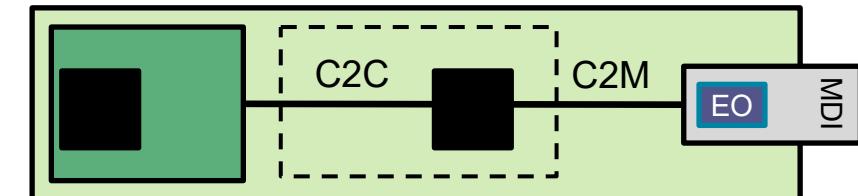
Type	IC	Reach	Power
Passive	None	~1m	
Active Electrical Cable (AEC)	Retimer		
Active Copper Cable (ACC)	Redriver		



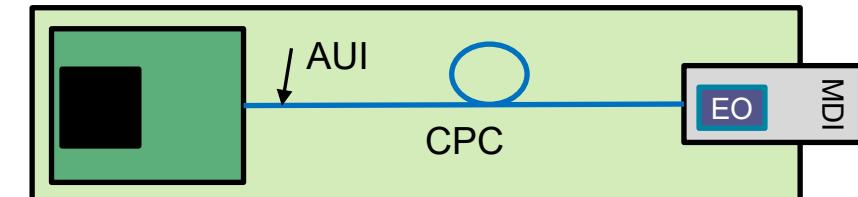
C2M Hosts for 400 G/lane

- Broader mix of host implementations than previous rates
 - PCB traces to front panel pluggable (FPP)
 - Co-packaged cables to FPP
 - Near-Package Optics (NPO)
 - Co-Packaged Optics (CPO)
- Electrical and optical integration becomes critical for achieving performance and reach targets

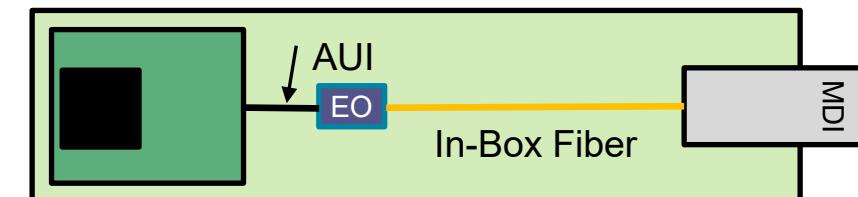
Traditional -
PCB Traces



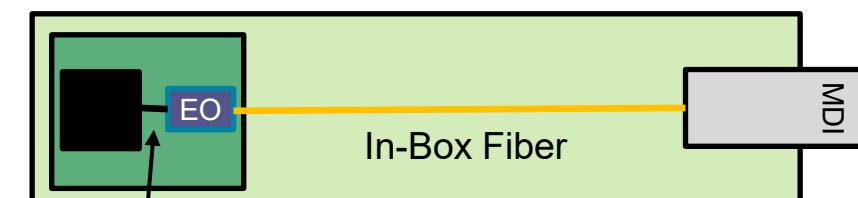
Co-Packaged
Cabling



Near Package
Optics (NPO)



Co-Packaged
Optics (CPO)



Electrical Interfaces: PAM4 or Not?

- Electrical modulation choice is highly dependent on the channel response:
 - Package, host traces or CPC assembly, front panel or CPO/NPO connector, cable assembly or backplane, etc.
- Every individual element in the channel has a dramatic effect on the overall end-to-end link performance
- There is no extra margin ☹ - “pennies in the sofa”

Key Questions for Electrical PAM-4/6/8

- **System Design:** How many 400 G/lane ports and what mix (copper vs. optics) of them will be in a switch, NIC, accelerator/xPU?
 - Will there be a change in the base assumptions of how to build a system?
- **Industry Readiness:** Will new electrical connectors and media meet performance targets at scale?
- **Modulation Alignment:** How critical is common coding for electrical and optical interfaces?
 - Are linear solutions (pluggable/co-packaged) viable at 400G/lane, and when?
- **Validation Tools:** Are test & measurement solutions prepared for PAM-4/6/8 at scale?

Optical Interfaces: Is There a Quick Start?

- Strong assumption regarding optical modulation
 - PAM4 modulation is the leading candidate
- Can existing building blocks (FEC) be assumed?
- High-radix use case assumes both CPO & pluggable implementations
- SMF is a benign channel for single-lane
 - 500m reach seems useful. Any power/cost/yield advantage to defining shorter (or longer)?
- Link methodologies (e.g. test methodologies) need early focus

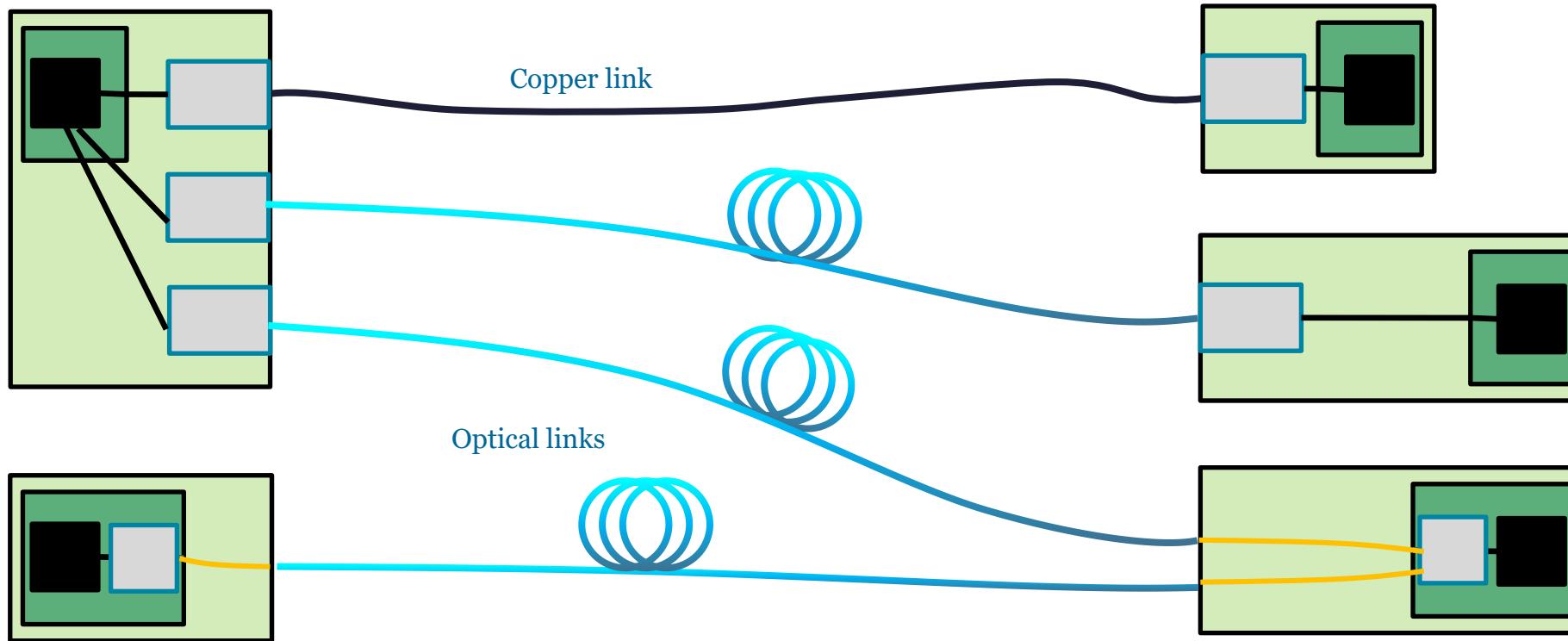
Key Questions for Optical

- **System Design:** Does CPO (in addition to pluggable) bring any new considerations? Interop needs to be independent.
- **Industry Readiness:** Will any new technologies or media meet industry ability to scale? The ecosystem matters.
- **Modulation Alignment:** How critical is common coding for electrical and optical interfaces?
 - Are linear solutions (pluggable/co-packaged) viable at 400G/lane, and when?
- **Validation Tools:** Are test & measurement solutions prepared for 400G optical?

FEC/PCS: Intersection of Electrical and Optical

- Historically, there was modulation commonality of optics and electrical
 - E.g. NRZ-to-NRZ, PAM4-to-PAM4
 - Enabled linear/un-retimed optical solutions
- Historically, the copper interconnect determined the FEC code
 - Copper required burst-tolerant FEC codes, e.g. RS(544, 514)
 - Optics used the same or added an inner FEC code, e.g. Hamming(128,120)
- Is RS(544) sufficient for 400G/lane, or should we proactively consider a clean sheet FEC approach?
- Does the existing FEC/PCS scale well for high-radix uses cases at the new signaling rate?
 - What about the latency for single-lane and two-lane cases?

Seamless Interoperability: An Ethernet Expectation



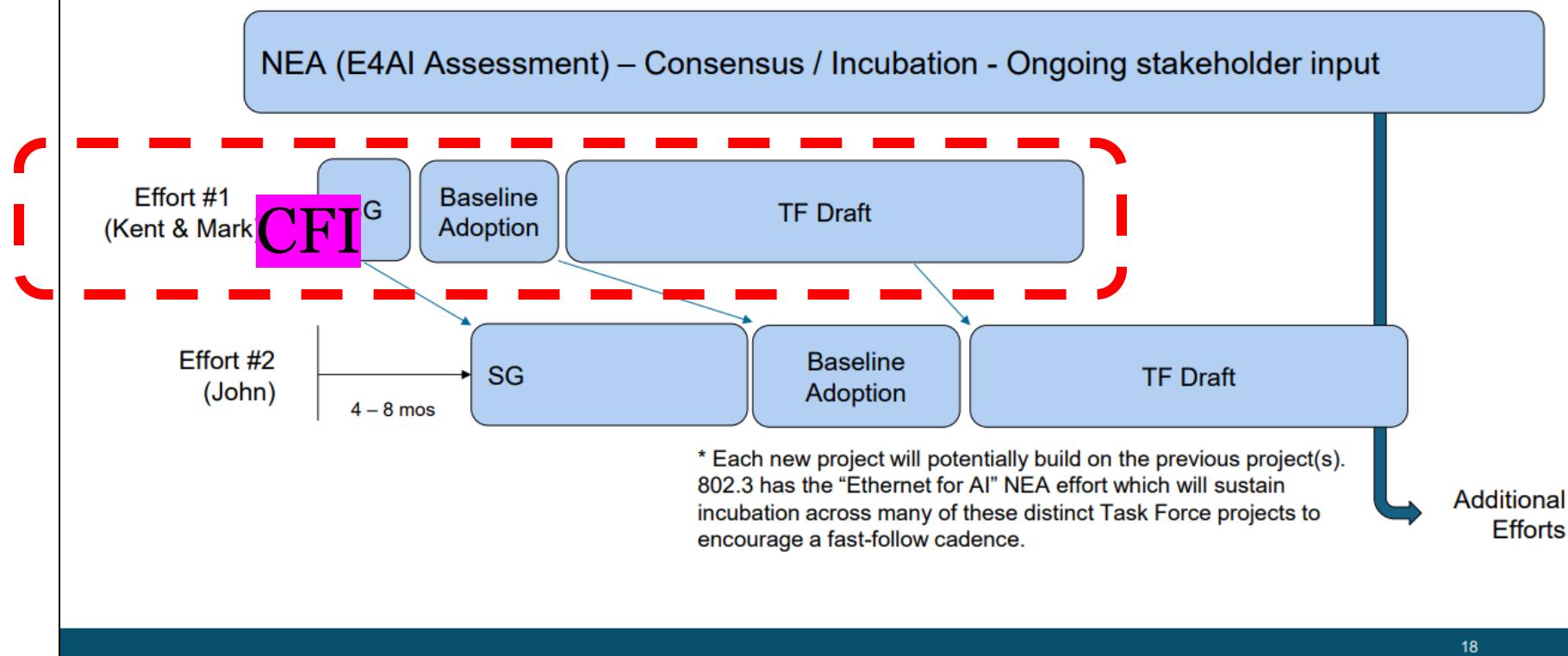
- Both copper and optical connections are essential for hosts
- Pluggable and CPO optics must work together cohesively

The Effort(s) Interconnect Implications Getting Started Now

Fast and Nimble!

Critical First Step Towards 400G/lane Standard

Moving Forward in IEEE 802.3



Anticipated 400G/lane Signaling Project Objectives

- Usual Foundational
 - Full Duplex, Ethernet frame format & size, FLR, etc.
- Existing Ethernet rates
 - 400GbE (x1), 800GbE (x2), 1.6TbE (x4)
- New 400 Gb/s per lane PHYs & Interfaces:
 - Copper cable and backplane - reach TBD (passive plus active)
 - Optical single-lane SMF (PSM) - reach <= 500m
 - Electrical C2M and C2C interfaces

Summary

- The Ethernet community must *quickly* respond to support the AI network time-to-market requirements and use cases
 - Make decisions (modulation, FEC, host type, etc.), refine as necessary
- 400G/lane technology will tightly integrate electrical, optical, and FEC/PCS domains.
 - Both copper and optical connections are essential for hosts
 - Pluggable and CPO optics must work together cohesively
 - The ecosystem matters
- March 2026 CFI for 400 G/lane signaling
 - Initial focus is 400G/lane copper and short-reach optical PHYs based on existing MAC rates

Thanks!