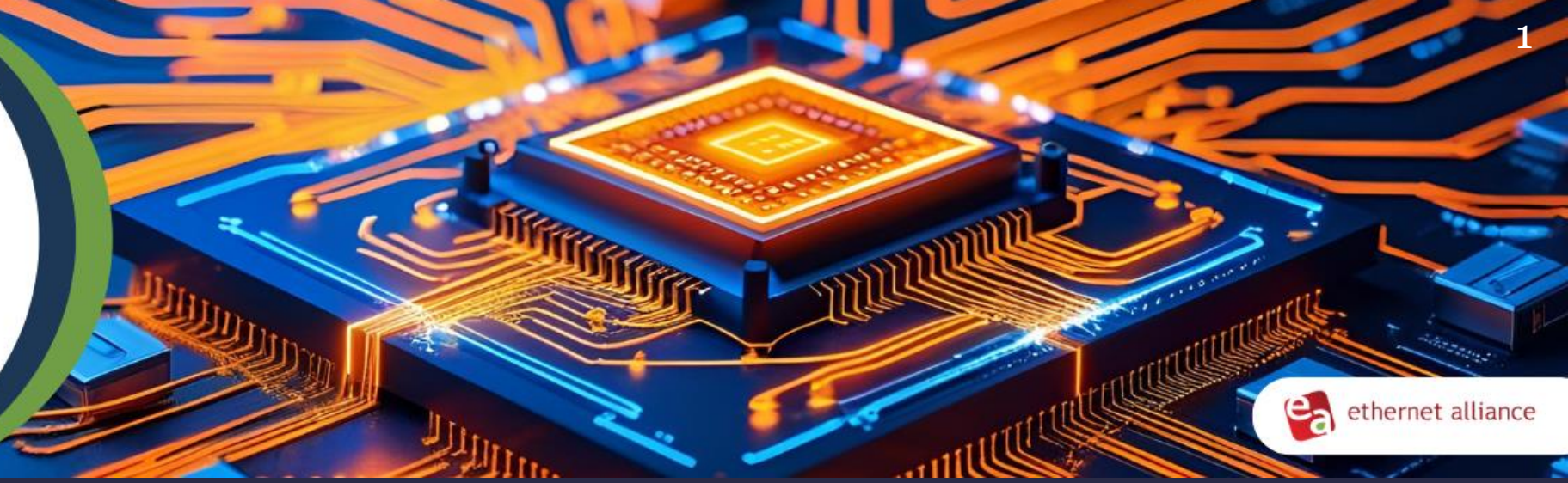
TEF 2025
Ethernet for AI

December 2-3, 2025
Hyatt Centric Mountain View, CA, USA



ethernet alliance

The Path to 448G in Support of Next Generation AI

OIF Update on the 448G Framework project

December 2-3, 2025

OIF

This presentation has been developed within the Ethernet Alliance, and is intended to educate and promote the exchange of information. Opinions expressed during this presentation are the views of the presenters, and should not be considered the views or positions of the Ethernet Alliance

Accelerating Market Adoption of Optical Networking Technologies

160+ Member Companies ▶ 25+ Years of Service ▶ Member Driven Global Organization

COHERENT OPTICAL

Multi-Vendor Interoperability in Client Form Factors

1600ZR+
- <1000km Multi-Span Coherent DWDM

1600ZR, 800ZR, 400ZR
- >80km Coherent DWDM

1600LR, 800LR
- <10km Coherent Point-to-Point

ELECTRO-OPTICAL

Energy Efficient Interfaces (EEI) –Low Latency/Optimized Energy Interfaces for AI/ML
- Compute Optics Interface (COI)
- Retimed Tx, Linear Rx (RTLR)
- External Laser Sources (ELSFP)
- Co-Packaged Modules (3.2T)

Common Electrical I/O (CEI)
- High-Speed Building Blocks
- 448G, 224G, 112G, 56G, 28G
- LR, MR, VSR, XSR+, XSR, MCM, Linear
- Protocol Agnostic Link Training

OIF

Identifies Industry Needs and Gaps

Publishes Implementation Agreements (specifications) (100+), Requirements and White Papers

Performs Interoperability Demonstrations (65+)

Advances industry consensus via workshops, webinars, etc.

MANAGEMENT

Common Management Interface Specification (CMIS)
- Single Solution Ranging From Copper to Coherent
- Simplified Bring up Between Host and Module
- Supports Standard and Custom Interfaces

Transport SDN APIs
- Automation, Programmability

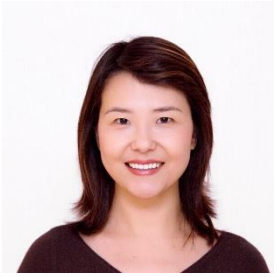
Enhanced Network Operations
- Artificial Intelligence
- Digital Twin
- DC Storage and Optical Multi-Layer Coordination

PROTOCOL

Flex Ethernet (FlexE)
- 800 Gb/s Ethernet PHY support

For more information, visit www.oiforum.com

Panelists



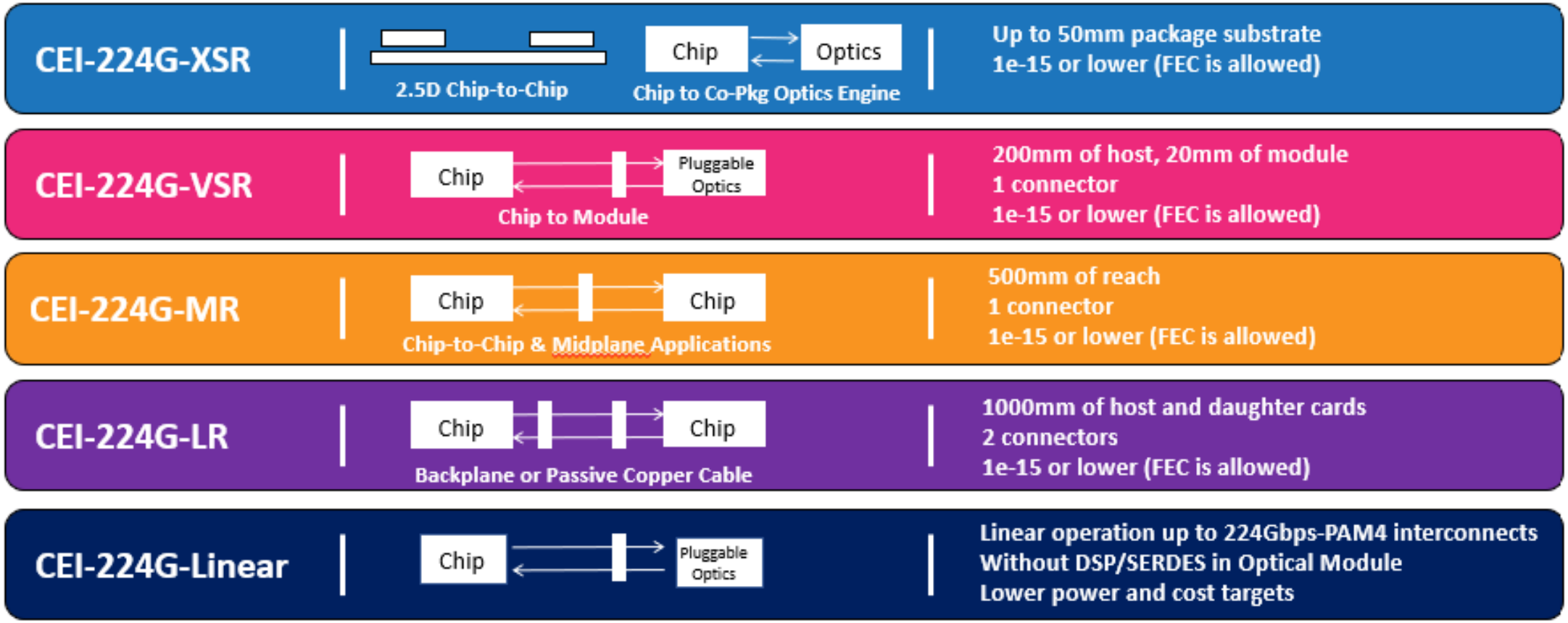
Cathy Liu
OIF Vice President
Distinguished Engineer, Broadcom
“Electrical Interconnection Considerations”

Mike Li
OIF Board Member
Fellow and Chief Technologist, Altera
“Electrical Channel and Modulation Considerations”

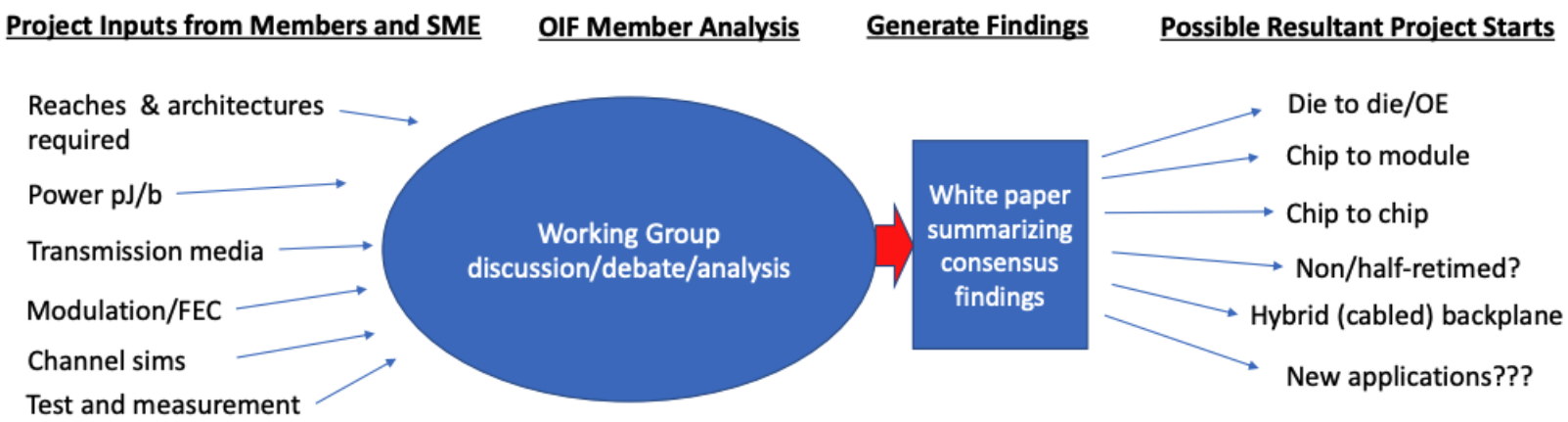
Jeff Hutchins
OIF PLL WG EEI Vice Chair
CTO Office, Ranovus
“Does Optics Have What is Needed For Scale-Up/Out Links?”

John Calvin
Senior Product Planner
Keysight Technologies
“Advances in Measurement Science”

OIF Delivers Interoperable Power Optimized Electrical Definitions



448G Next Generation CEI-448G Framework



OIF CEI-448G Framework Project Start in August 2024

Access the OIF 448G Framework Document here:

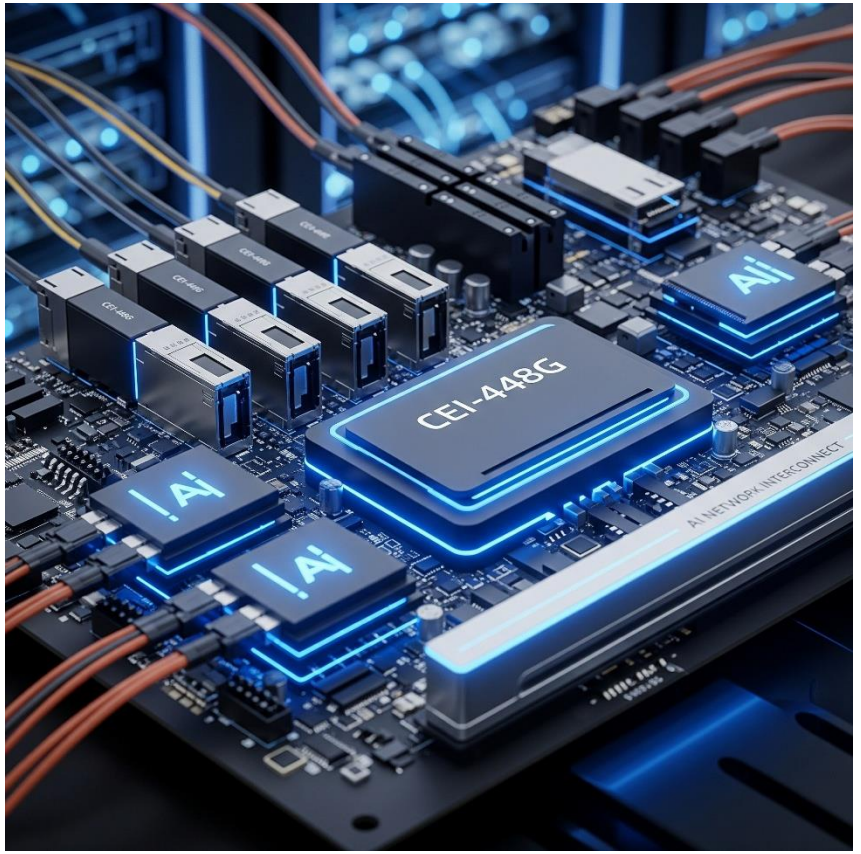
https://www.oiforum.com/wp-content/uploads/OIF-FD-CEI-448G-01.0.pdf

Electrical Interconnect Considerations

Cathy Liu
OIF Vice President
Distinguished Engineer, Broadcom

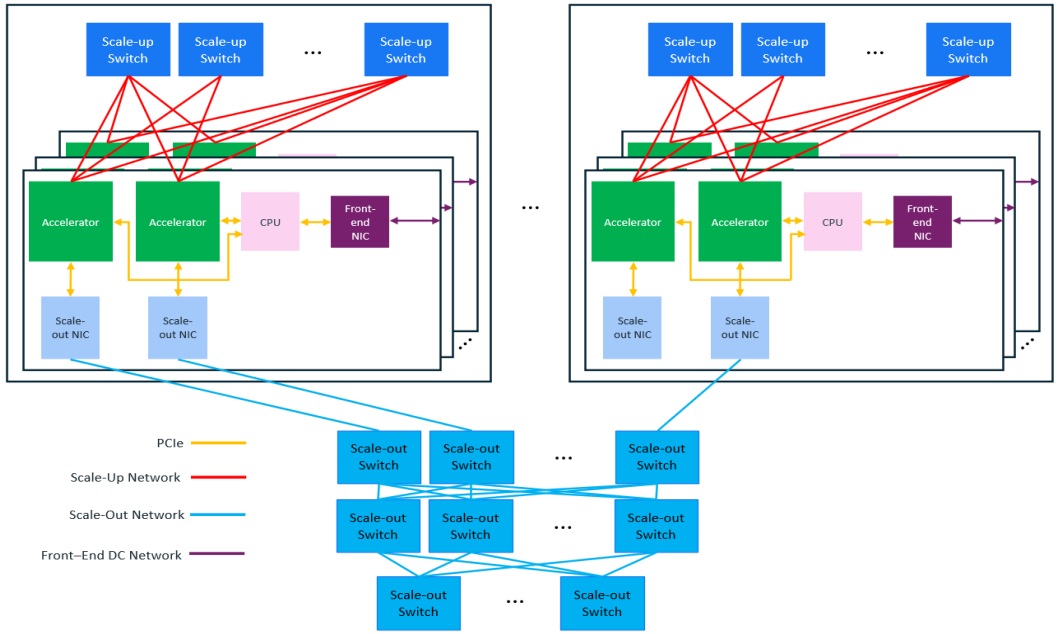
Agenda

- The shift to 448G to meet AI scaling challenges and bottlenecks
- Key challenges and potential solutions for 448G electrical interconnect
  - Cost, power and electrical link reach
  - Channel requirements and characteristics
  - Modulation, equalization, and FEC/latency
- CEI-448G interconnect application interfaces



Shift to 448G

- Interconnects are an essential part of AI infrastructure
- Copper remains as primary interconnect for scale-up network today
- To keep pace with the growth in AI model parameters size, OIF created the CEI-448G framework



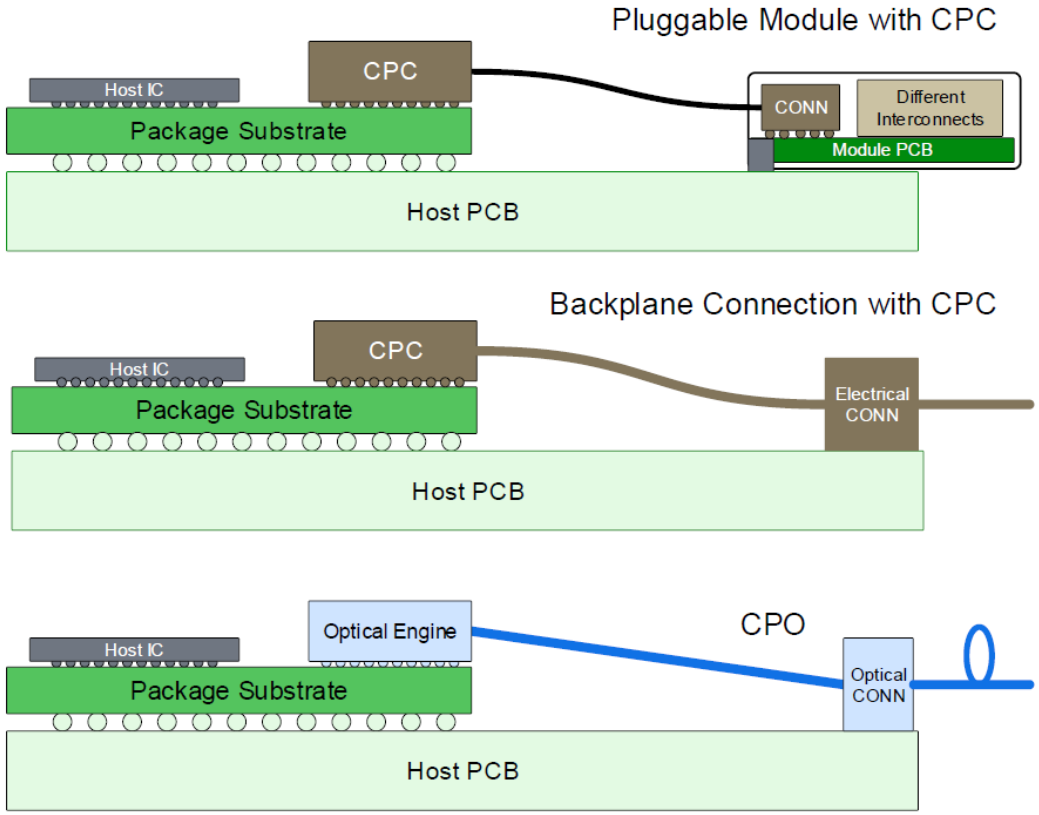
	Scale-Up		Scale-Out	
	State of Art Today	**Next Generation**	**State of Art Today**	**Next Generation**
# of Accelerator Nodes	~100	~1k	100k+	>>100k
Physical Size	Rack	Rack to Row	Datacenter	Datacenter
Network Properties	Lossless, Low Latency		Large scale	
Primary Interconnect Type	Passive PCB Twinax Backplane: within rack AEC: between adjacent racks	Twinax Backplane: within rack AEC: between adjacent racks Optical: within row	Optical	Optical

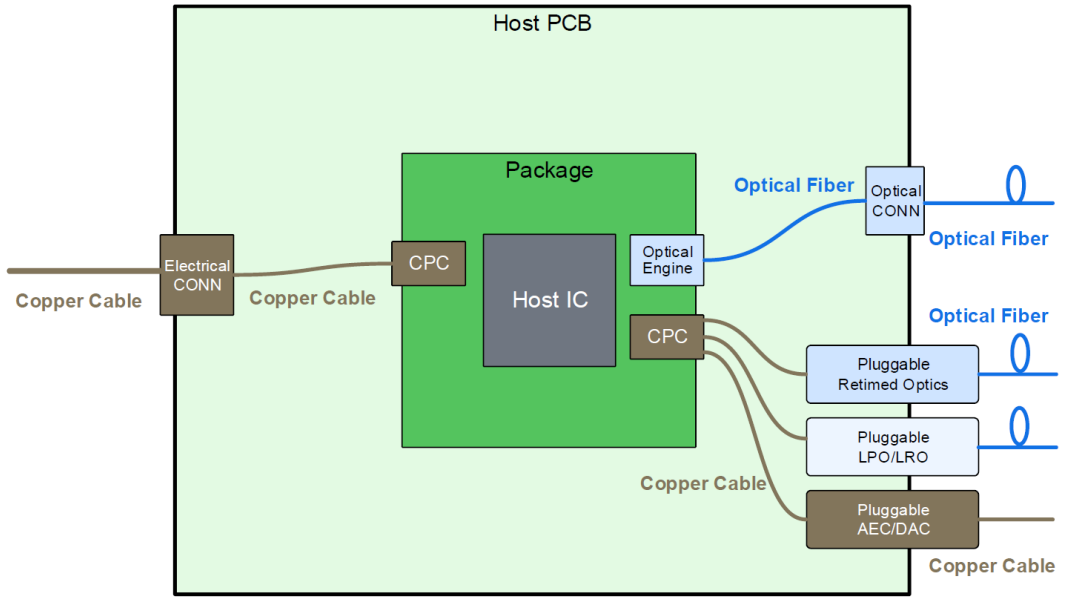
Cost, Power and Electrical Link Reach

- Achieving comparable reach to 224G at 448G is exceptionally challenging
- The increased Nyquist frequency for 448G poses significant challenges for bandwidth-limited copper interconnects
- Power consumption is a critical constraint; balancing longer reach with its impact on interconnect power is crucial
- Tail latency significantly hinders AI applications, especially in distributed training and inference, requiring careful design consideration

OIF CEI projects	CEI-56G-LR	CEI-112G-LR	CEI-224G-LR	CEI-448G-LR
Timeline	2014-2017	2017-2021	2021-	2026-
Ethernet rate	50/100/200G	100/200/400G	200/400/800/ 1600G	400/800/1600G/3200G
Switch capacity	12.5T	25T/50T	50T/100T	100T/200T
Per-lane data rate	56 Gbps	112 Gbps	224 Gbps	448 Gbps
Modulation	PAM4	PAM4	PAM4	TBD
Insertion loss	30dB at 14GHz ball-ball	28dB at 28GHz ball-ball	40dB at 56GHz bump-bump	TBD
Reach objectives	3m copper cable	2m copper cable	1m copper cable	TBD
Pre-FEC BER target	1e-4	1e-4	1e-4	TBD
SerDes architecture	Analog/DSP	Analog/DSP	DSP	TBD

Typical 448G Electrical Applications





CPC: Co-packaged Copper

LPO/Linear: Linear Pluggable Optics

DAC: Direct Attach Copper Cables

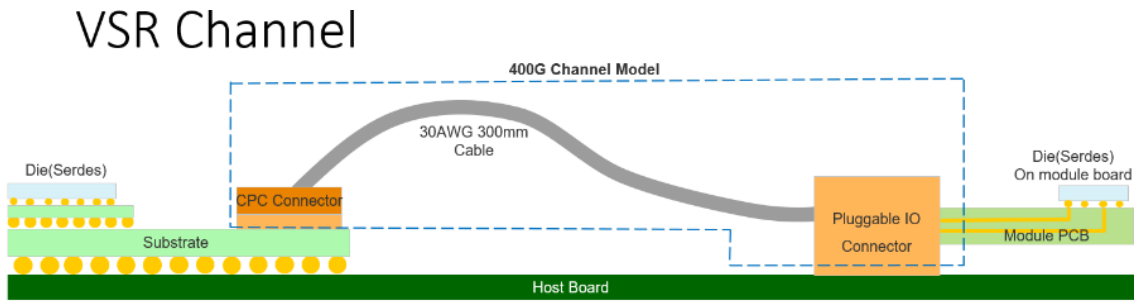
CPO: Co-packaged Optics

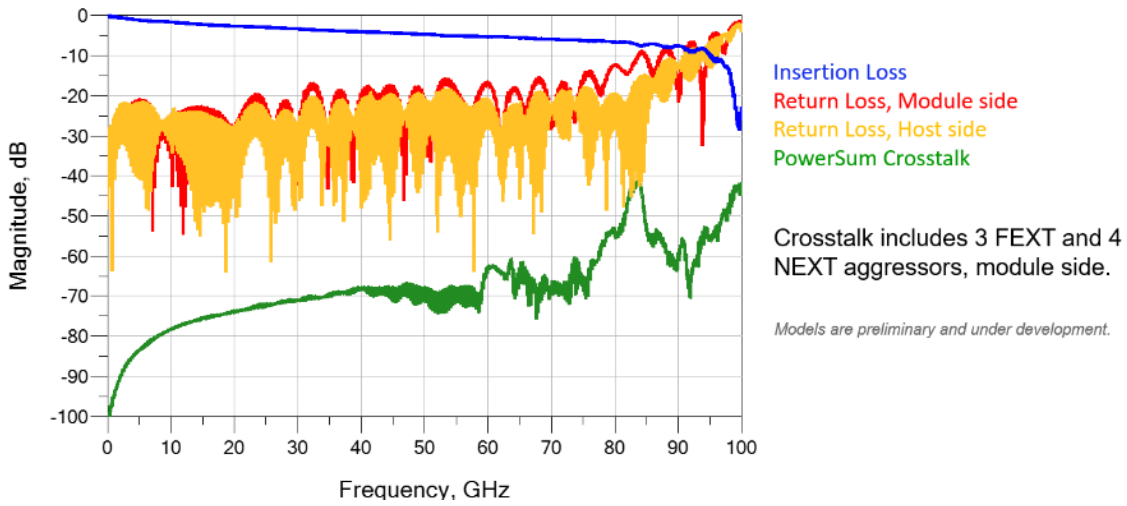
LRO/RTLR: Linear Receiver Optics

AEC: Active Electrical Cables

Channel Requirements and Characteristics

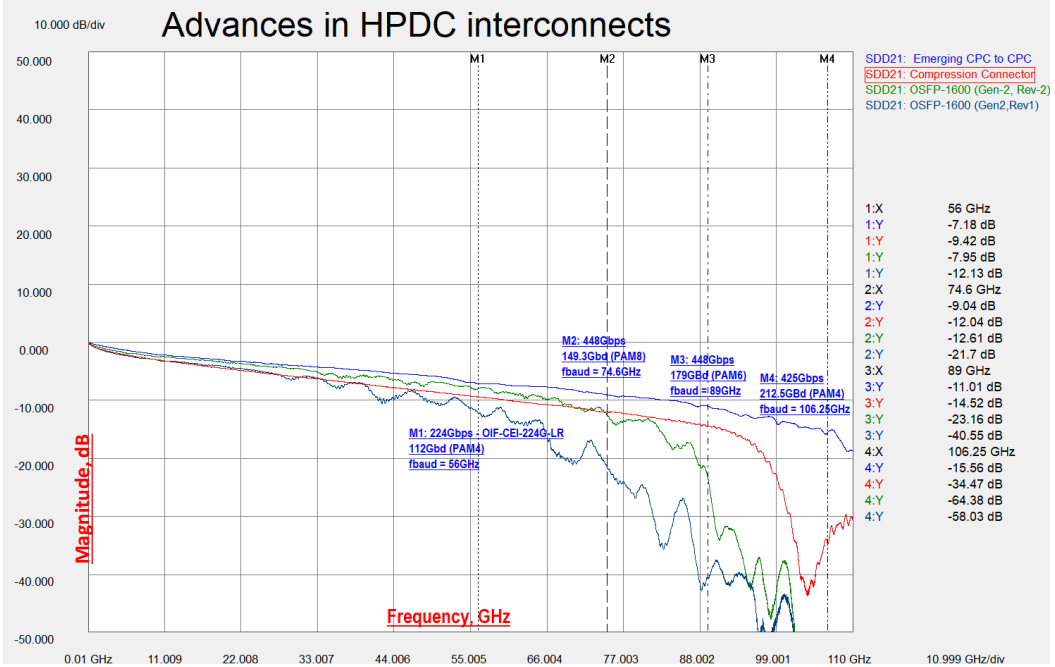
- Increasing data rates lead to degradation in SNR due to increased conductive and dielectric losses, and noise from reflections and crosstalk
- Increased I/O density exacerbates crosstalk concerns
- Intra-pair skew can amplify jitter and inter-symbol interference, degrading the eye diagram
- Current channel bandwidth is limited to approximately 90 GHz, largely due to connector technology, making PAM4 challenging for 448G





Channel Advancements

- Meanwhile, emerging interconnect technologies and ongoing advancements in connector design offer promising pathways to overcome these bandwidth limitations.
- However, what if these existing connector/channel bandwidth limitations persist longer?
- To meet fast pace of AI network demanding
  - Short-term: Maximize near term infrastructure
    - Requires higher order modulation
  - Mid-term: Address channel limitations without full-scale replacement
    - Use PAM4 where possible, e.g. XSR
    - Use higher order modulation where required, e.g. LR
  - Long-term: Full-scale hardware transition
    - Full transition to lowest possible modulation
    - Use higher order modulation for longer reach or faster speed (e.g. > 448 Gbps)



Potential Solution Spaces (Modulation, FEC …)

- If channel bandwidth remains limited to ~90 GHz, higher-order PAMn modulations (like PAM6 or PAM8) may be necessary, but
  - This creates mismatches with IMDD optical PMD modulation and impacts backward compatibility
  - This implies that 448G linear pluggable optics (LPO) will not be possible
  - A stronger FEC could be necessary for **448G electrical link** to offset SNR penalty
- FEC can be enhanced by
  - Adding redundant symbols (e.g., an inner code)
    - Like 200G IMDD optics inner code
    - However, this increases the overall baud rate and consumes more bandwidth
  - Expanding Modulation Constellation Space (e.g., coded modulation)
    - This will not increase the overall baud rate and achieve better spectral efficiency
    - However, more complicated DSP detection is needed

448G Interconnect Applications

Interconnect Application	Distance Up To	Types of interfaces	Potential CEI projects
Die to Die in a Package	~25mm	Electrical	XSR
Die to Optical Engine in a Package	~50 mm	Electrical	XSR/XSR+, Linear, RTLR
Chip to nearby optical Engine	~150 mm	Electrical	XSR/XSR+, Linear(?), RTLR(?)
Chip to pluggable module	~250 mm	Electrical	VSR, Linear(?), RTLR(?)
Chip to chip within PCBA	~50 cm	Electrical or Optical	MR
PCBA to PCBA across a backplane/midplane/cable	~1 m	Electrical or Optical	LR
Chassis to Chassis within a rack	~1 m	Electrical or Optical	LR

- CEI-448G-FD identified potential CEI-448G electrical interconnection applications

Electrical Channel and Modulation Considerations

Dr. Mike Peng Li
OIF Board Member
Fellow and Chief Technologist, Altera

Agenda

- PAMn modulation considerations for 448G
  - Modulation vs SNR/UI/jitter
  - Modulation vs channel IL
- PAMn SERDES and package at 448G
- Latest CPC technology and E2E channel/link at 448G
- Summary

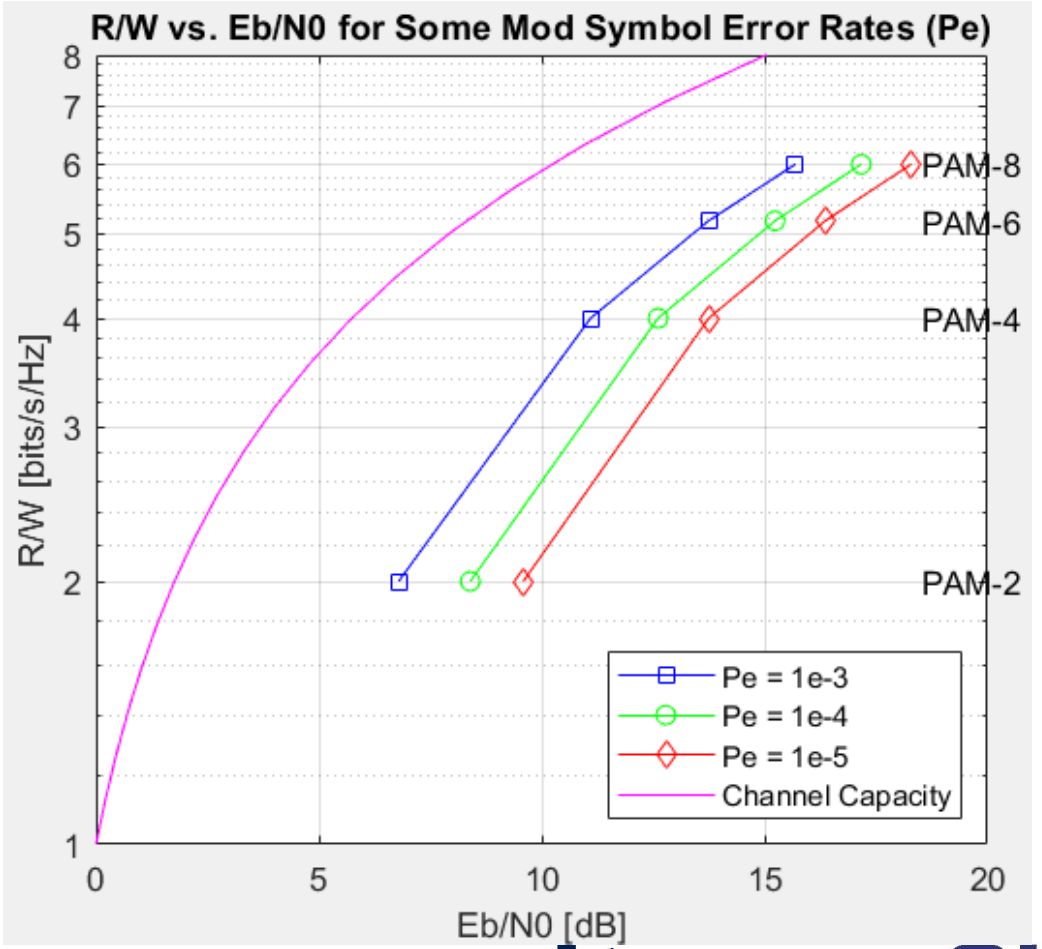
Comparisons of 448 Gbps PAMn Modulations

Data Rate (Gbps)	448	448	448	448	448	448
PAMn Levels	4	5	6	7	8	16
Bit per symbol	2.00	2.32	2.50	2.81	3.00	4.00
Symbol Rate (Gbps)	224.00	192.94	179.20	159.58	149.33	112.00
UI (ps)	4.46	5.18	5.58	6.27	6.70	8.93
Nyquist Freq (GHz)	112.00	96.47	89.60	79.79	74.67	56.00
SNR Delta (dB)	0.00	-2.50	-4.44	-6.02	-7.36	-13.98

PAMn on BW Efficiency Plane

- Different trajectory of different modulation on Bandwidth Efficiency Plane

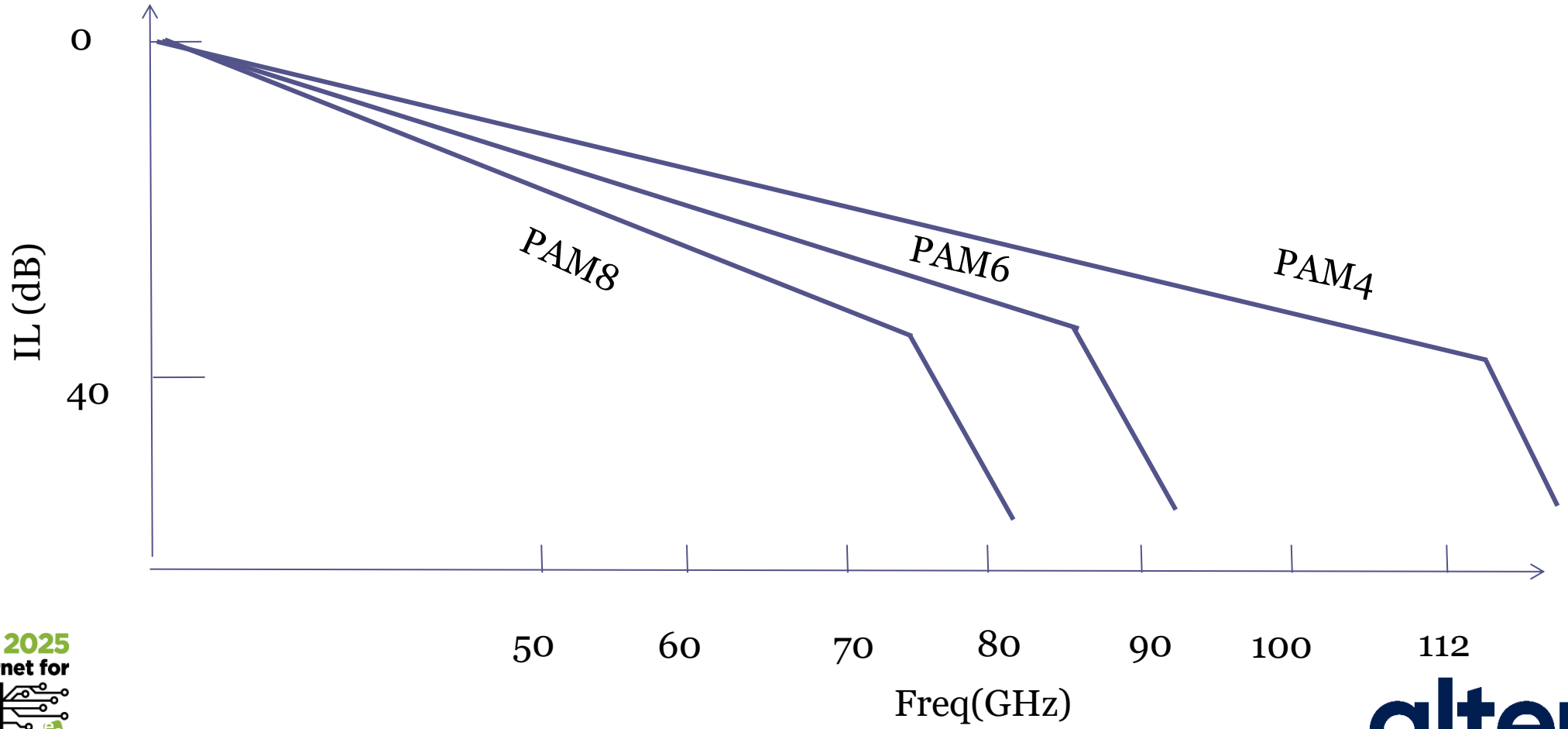
- PAMn and their distance from channel capacity are the focus
  - Each PAMn location on BW Efficiency Plane depends on its symbol error probability (Pe)
  - Higher order PAMn of the same Pe requires larger Eb/No for a given peak (or peak-to-peak) voltage and noise level
  - The lower Eb/No (normalized signal-to-noise ratio (SNR), the closer to channel capacity and the higher Pe
  - The closer to channel capacity, the more complex and longer latency FECs are required for reliable communication, which is not liked by AI/ML



R/W defines the bandwidth efficiency which is the ratio of the maximum data rate (R) to the available bandwidth (W)

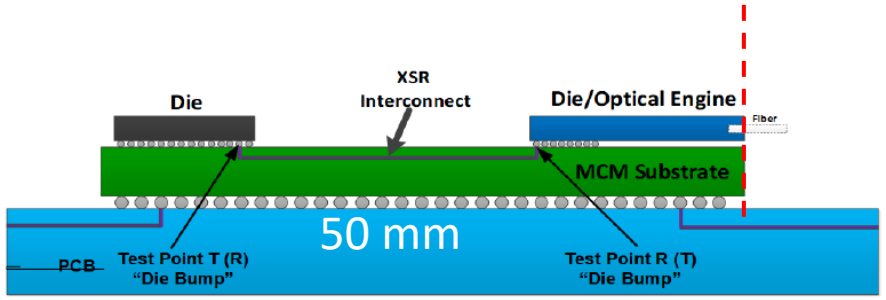
448G Channel IL vs PAMn

- PAMn choice critically depends on the channel bandwidth

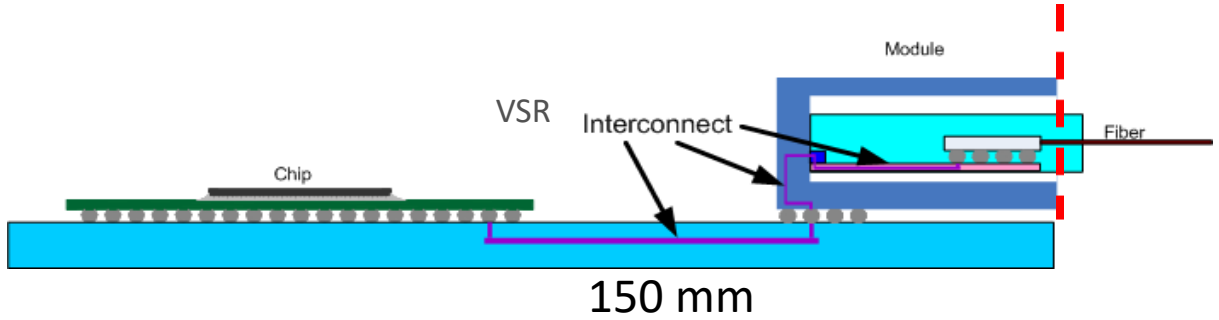


448G Chip-to-OE/Module Modulation Considerations

XSR



VSR



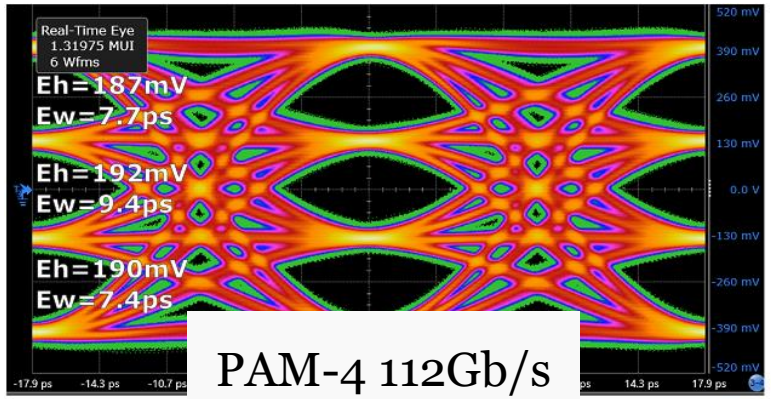
	e-XSR	e-VSR/MR	o-DR	Notes
224G	**PAM4**	**PAM4**	**PAM4**	
448G -PAM4 elec -PAM4 opt	**PAM4 -Desirable for elec to opt alignment -Unknown if production is feasible**	**PAM4 -Desirable for elec to opt alignment -Unknown if production is feasible**	**PAM4 -Desirable for elec to opt alignment -Desirable for better SNR**	**vs PAM6/8 elec • e-o compatibility • Enable LPO/lower power/lower cost • Lower latency in optical links/backward compatibility • Production feasibility under investigation • Elec channel reach is compromised**
448G -PAM6/8 elec -PAM4 opt	**PAM6 -Undesirable for elec to opt alignment**	**PAM6/8 -Undesirable for elec to opt alignment -Improved production feasibility**	**PAM4 -Undesirable for elec to opt alignment -Doesn't get to the lowest power (LPO)**	**vs PAM4 • Better TTM • No e-o compatibility without gearbox • No LPO/lower power/lower cost • Optimized Elec channel reach**

448G SERDES

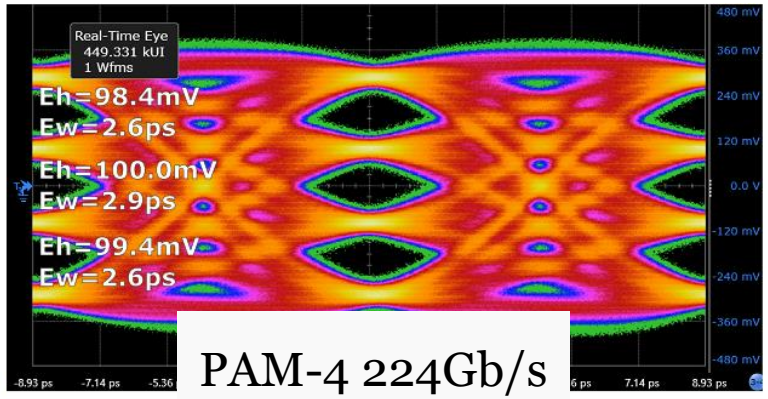
- With:
  - Advanced architecture, including advanced digital-to-analog converter (DAC)-based transmitter (TX), analog-to-digital converter (ADC)- based receiver (RX), advanced Analog Front End (AFE)
  - Efficient SNR-oriented calibration of ADC
  - Efficient convergence and adaptation algorithms
  - Advanced process nodes (e.g., <=N3/N2, <=18A)
- 448G-PAM4/PAM6 SERDES are feasible

SERDES ADC/DAC Arch for Dual PAM4/PAM6

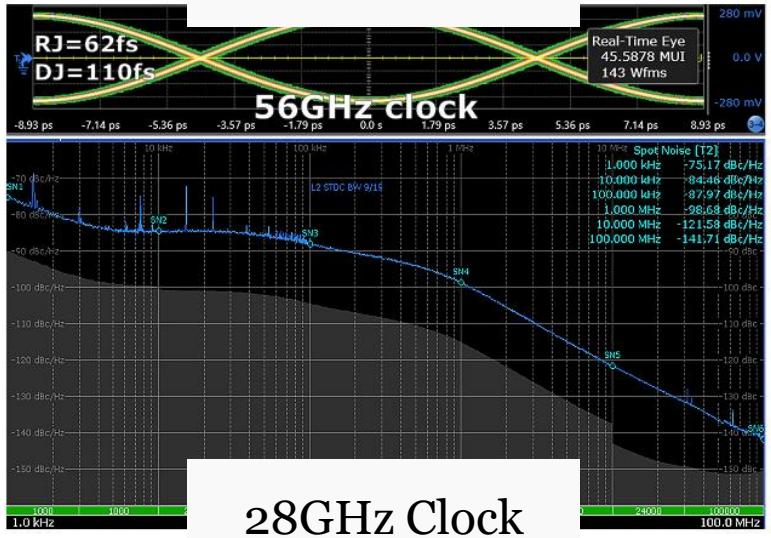
- Demonstrated at 224 Gbps and extendable to 448 Gbps



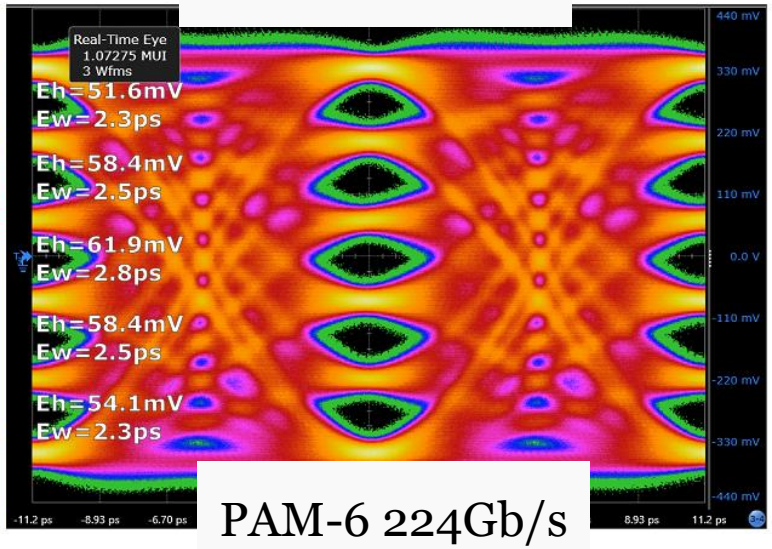
PAM-4 112Gb/s



PAM-4 224Gb/s



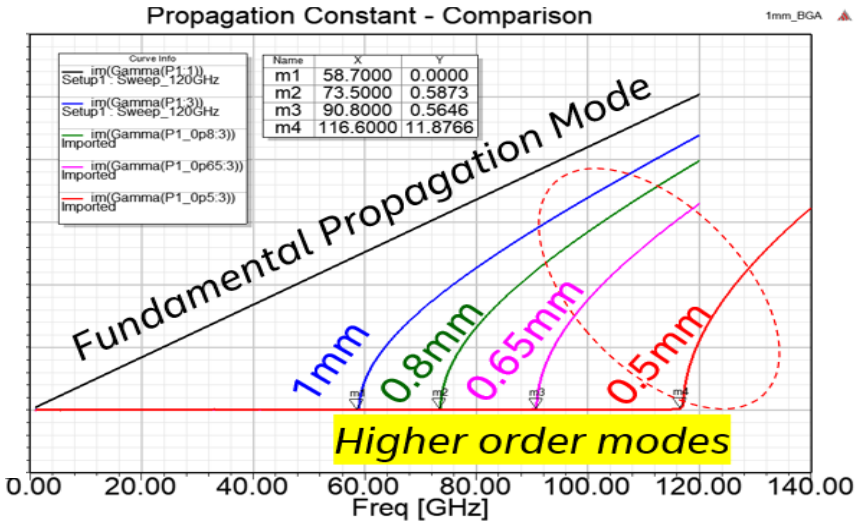
28GHz Clock



PAM-6 224Gb/s

448G Package

- Package BW depends on ball pitch
  - 112G (PAM4): ≤ 1mm
  - 224G (PAM4): ≤ 0.8mm
  - 448G (PAM4): ≤ 0.5mm
- **Package ball pitch of <= 0.5 mm is available today**



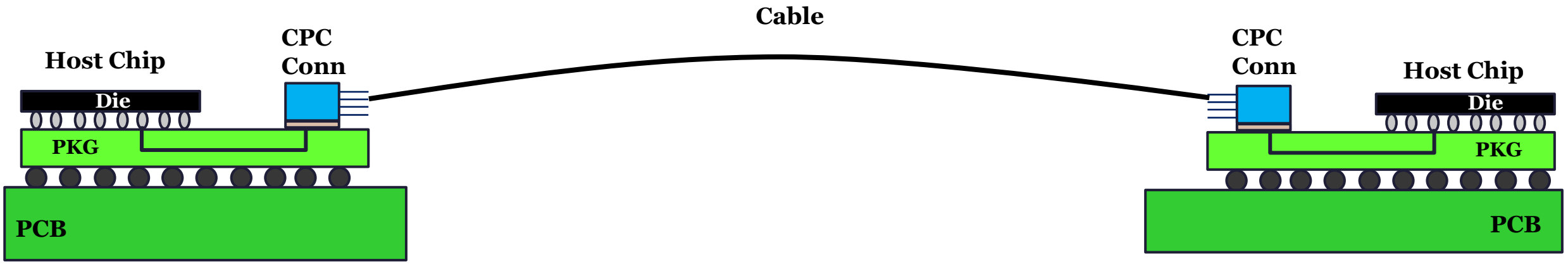
Cut-off frequency of BGA ball pitch

BGA pitch	1.0mm	0.8mm	0.65mm	0.5mm
Cutoff Frequency	58GHz	72GHz	90GHz	115GHz

	224G		448G			
Modulation	PAM4	PAM6	PAM4	PAM6	PAM8	PAM16
Nyquist Freq, GHz	56 GHz	44.8 GHz	112 GHz	89.6 GHz	74.67 GHz	56 GHz

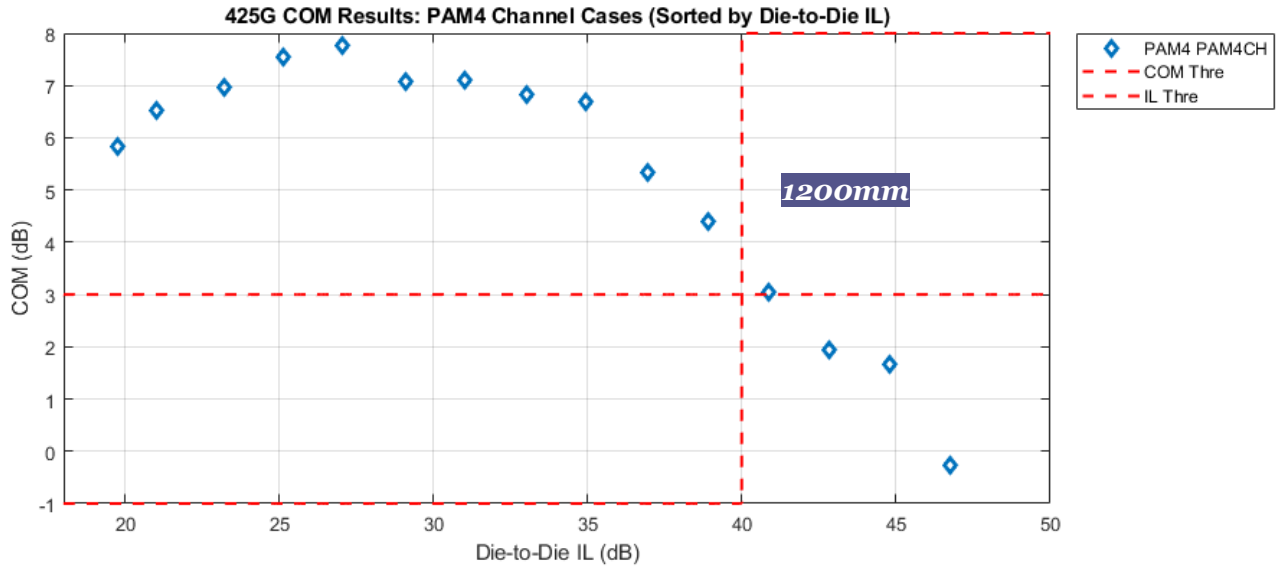
- PKG can potentially support 448Gbps-PAM4 signaling, with < 0.5 mm pitch, ball structure, advanced materials/stack ups (e.g., skip layer)

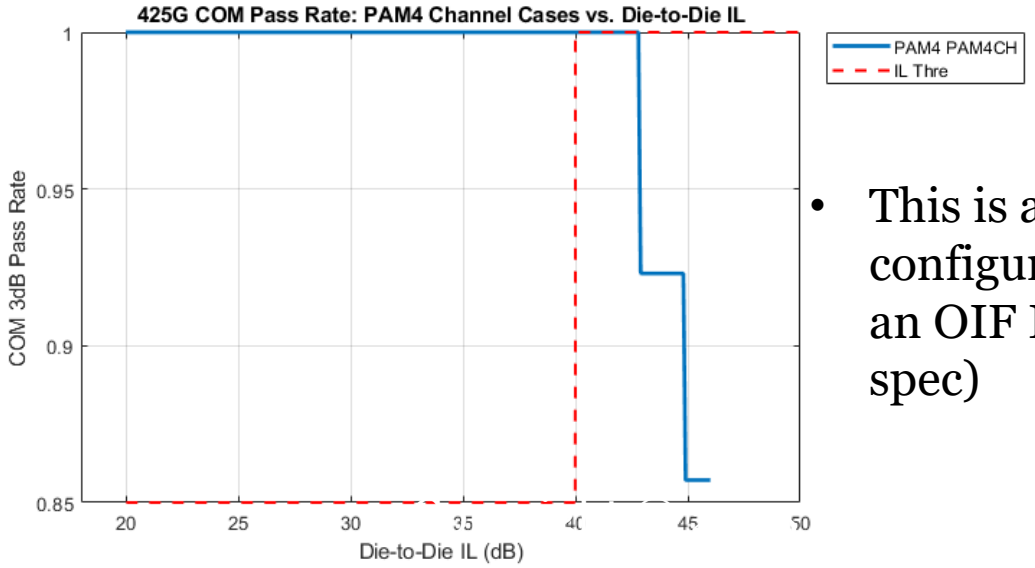
A 448G Electrical Cable Link System with CPC Connector



- 31 AWG cable with Luxshare CPC connector is used for this study

425 Gbps (Enet)-PAM4 COM Simulation Results: w E2E CPC Channels w/XTLK

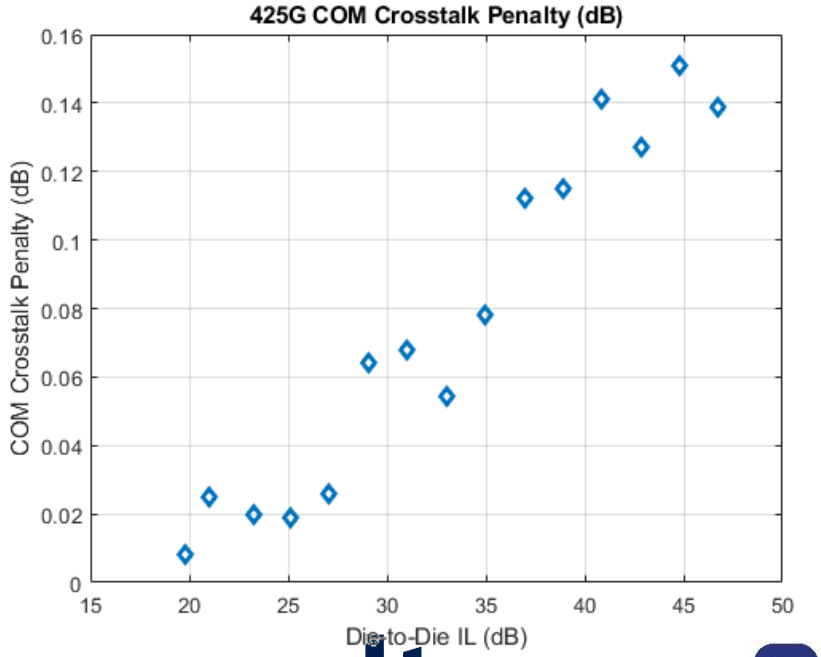




- This is a projected 448G COM configuration and analysis (not an OIF IA COM configuration spec)

- COM has healthy margin (1 –5 dB) when IL < 40 dB
- COM decreases with increasing die-to-die IL and cable length when IL >= 27 dB.
  - Last passing channel: 1200 mm (marginal)

- IL limit target based on 3dB COM pass rate
  - ~41dB



A Projection of OIF CEI-448G IAs and Characteristics (As of Dec, 2025)

Parameter	XSR	VSR	MR	LR	Linear
Data Rate (Gbps)	288 – 462	288 – 462	288 – 462	288 – 462	288 – 462
Post/Pre FEC BER (max)	1E-15/<1e-6(?)	1E-15/5e-5(?)	1E-15/5e-6(?)	1E-15/1e-4(?)	1E-15/2e-4(?)
Distance (max)	50 mm	220 mm	500 mm	1000 mm	120 mm
Interconnect	PCB+ 0 connector	PCB + 1 connector	PCB + 1 connector	PCB + 2 connectors	PCB + 1 connector
Insertion Loss (dB) (at $f_{N,}$ bump-bump)	~15	~30/35	~30/35	~35/40	~22
Modulation	PAM4	PAM8/6/4?	PAM8/6/4?	PAM8/6/4?	PAM4
Sys Power Target (pJ/b)	0.5	0.8	1.8	2.5	<2.5
FEC	Y	Y	Y	Y	Y

Power estimates assumes process technology in 2026-2027 (e.g., N2, 18A, 16A, 14A)

- E2E channel can support PAM8, PAM6 and PAM4 modulations
- Optical with PAM4 modulation

Summary

- PAM4 has served well for OIF CEI-56/112/224G, Ethernet 53/106/212G, and has been the dominate modulation for the ecosystem since 56 Gbps
- 448G-PAM4/6/8 SERDES are feasible with advanced process nodes (e.g., <=N3/N2, <=18A)
- Advanced package technologies supporting 448G-PAM4/6/8 signaling based on a pitch < 0.5 mm, along with advanced materials, ball structure, and stack-ups (e.g., skip-layer) have been simulated
- Latest CPC and associated passive cable technology supporting a reach up to 1.2m with 448G-PAM4 demonstrated via simulation
- 448G Optimal modulation (e.g., PAM4 vs PAM6 vs PAM8) depends on
  - End user TTM, power/cost, performance/latency requirements
  - Promising progress is being made across multiple connector/channel suppliers to support the system tradeoffs of PAM4 vs PAM6 vs PAM8
- PAM4 can enable low power XSR and LPO
- Lots of interesting and challenging work ahead in developing next gen 448G electrical I/O technologies and specifications

Does Optics Have What Is Needed For Scale-Up/Out Links?

Jeff Hutchins
OIF Physical & Link Layer Working Group Energy Efficient Interfaces (EEI) Vice Chair
Dir Optical Technologies, CTO Office, Ranovus

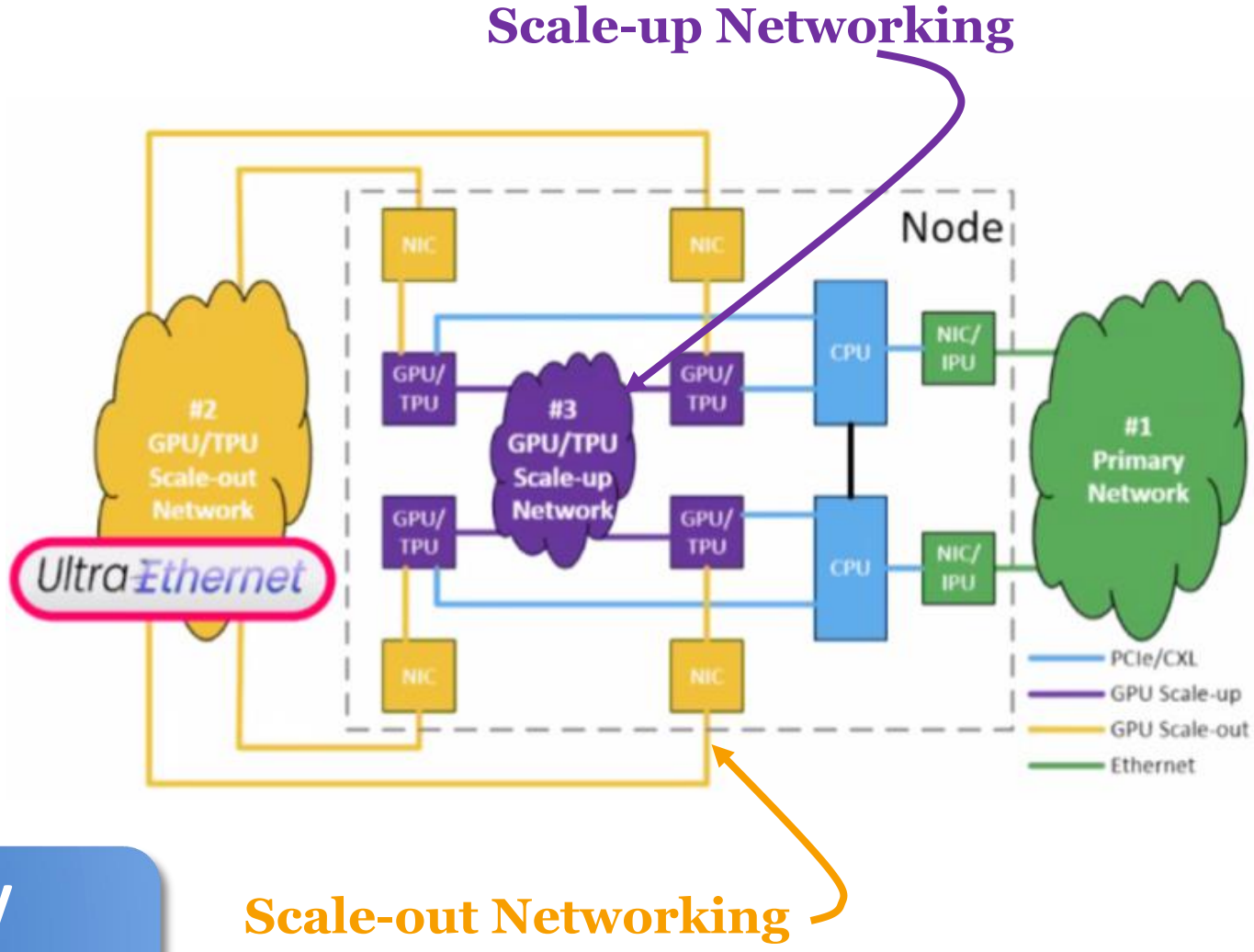
Scale-out & scale-up requirements from hyperscalers

Scale-out links

- Reaches of 100s of meters
- Currently using pluggable optics

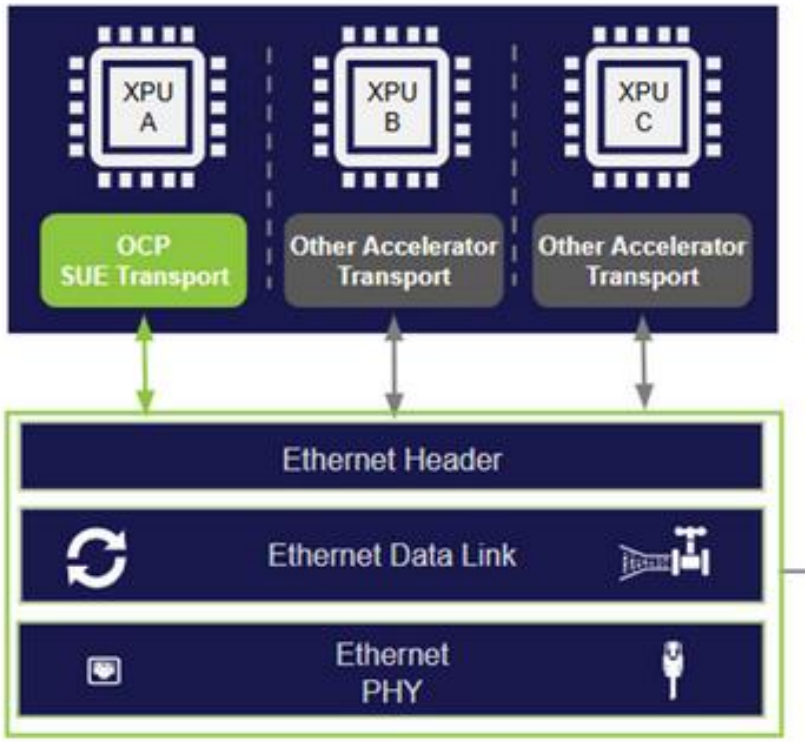
Scale-up links

- Reaches ≤ 20 meters
- ~ 10x the BW of scale-out
- More sensitive to latency
- Currently using passive copper



Energy efficiency is a key requirement for training Pods

Scale-out & Scale-up links will both leverage Ethernet



Enables innovation in the upper layers

ESUN standardizes the lower layers

OCP's ESUN Announcement

Scale-up interconnect will leverage Ethernet's lower layers

- **PCIe based links have been used for scale-up**
- **Now two important scale-up protocols:**
  - NVLink switching solutions
  - Ethernet based switching solutions like UALink, UEC, SUE-T, & recently ESUN
- **ESUN (Ethernet for Scale-up Networking)**
  - Announced at OCP October 2025
  - Enables a platform for open systems
  - Enables interoperability of xPU network interfaces and Ethernet switch ASICs
  - Aligned with UEC and IEEE802.3
  - ESUN will encourage diverse implementations and drive rapid adoption across the industry

Scale-up link bandwidth

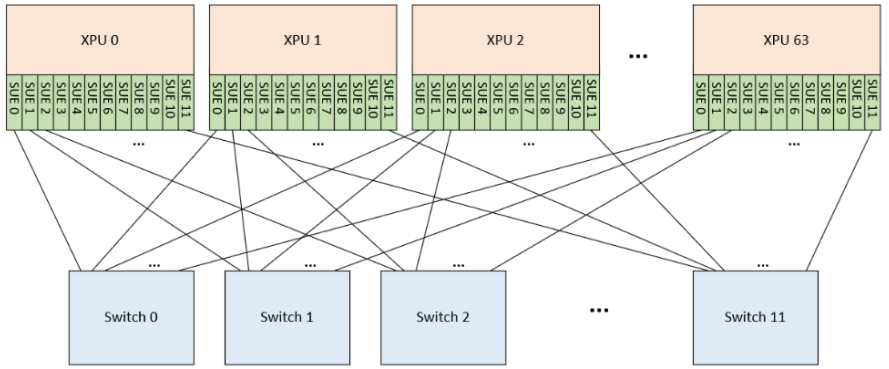
Every compute element connects to each switch creating a full mesh

Think of each link as a pipe to be filled

Today's systems use 400G pipes

- 2x 200G copper cables

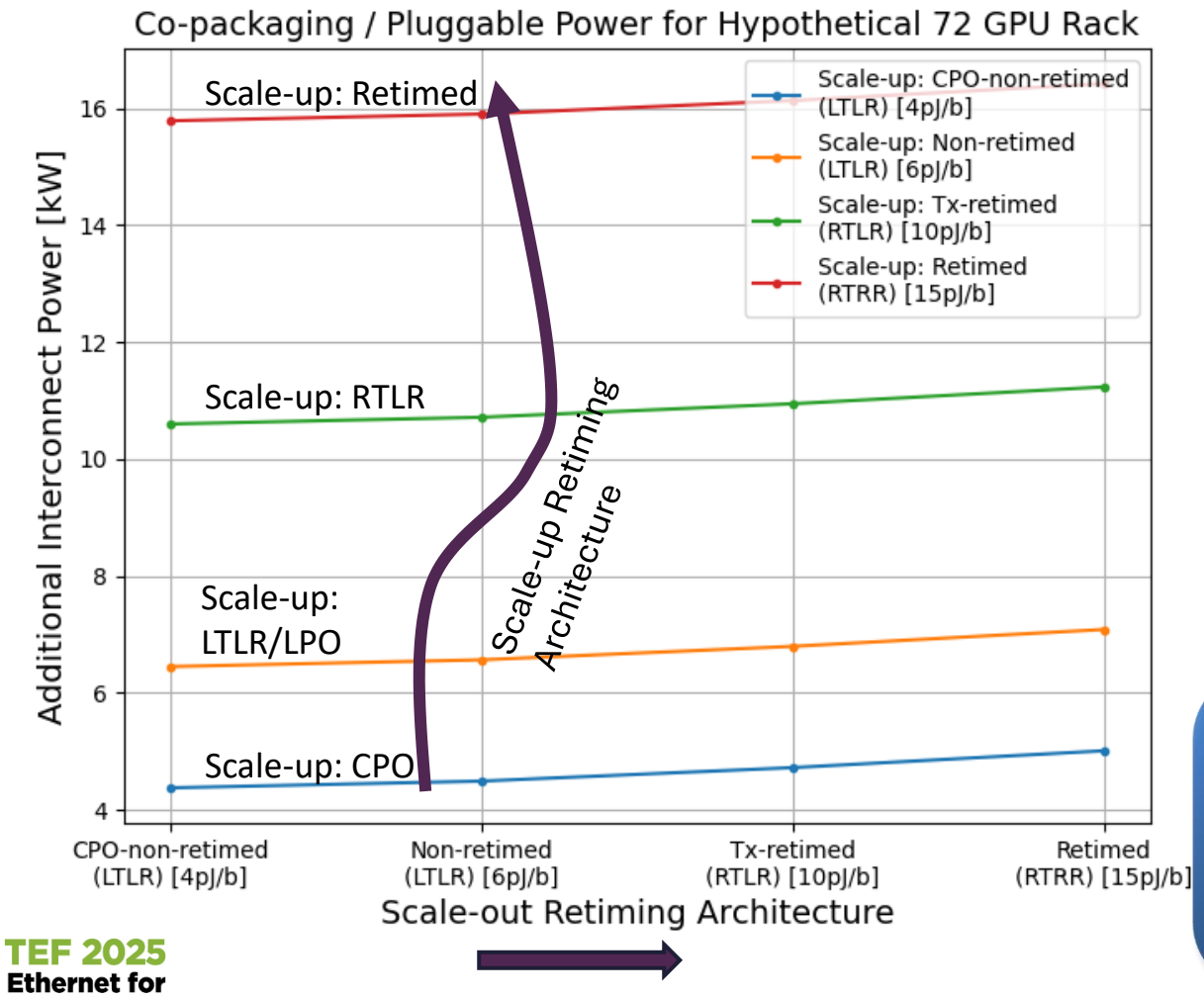
A future generation will need 800G pipes



Scale Up Ethernet Framework, Scale-Ethernet-RM102.pdf (June 13, 2025), https://docs.broadcom.com/docs/scale-up-ethernet-framework

A pipe can be filled with either one or more lanes and may carry bidirectional traffic

Large scale-up systems benefit from energy efficiency



- **Scale-up networking bandwidth is about ~10x that of scale-out networks**
- **Scale-up dominates the rack interconnect power consumption**
- **The lowest power solutions for optical connectivity will leverage co-packaging or linear/LTLR/LPO for scale-up**

Scale-up dominates the rack interconnect power, energy efficient solutions (CPO, LTLR) are lowest power

Reliability (link & hardware) are key requirements

Link reliability (packet loss) is key metric for scale-up

- Corrupted packets consume link bandwidth with retries
- CPO: Meta [1] reported no UCWs (uncorrectable code words) for > 1e6 400G-port-device-hours for a CPO switch

> *"Additionally, our measurements from the long-term reliability test infrastructure show no UCWs for over 1 million 400Gbps port device hours of continuous operation."*

[1] ECOC25, Tu.01.03.3: Co-packaged Optics Technology Evaluation for Hyperscale Data Center Fabric Switches, Siamak Amiralizadeh et. al;, Oct 2025, Meta

Hardware reliability is also a key metric for scale-up

- Due to the nature of AI Pods computation, failures necessitate a stop/restart
- Improved reliability is needed for scale-up, especially if inside the "box"
- Highly integrated solutions are anticipated to be more reliable
- Reliable solutions will likely leverage the IC industry's fabrication & packaging

Both hardware & link reliability is key for scale-up

Technologies for 400G pipes

Non-silicon materials for 400G serial PAM4

- InP, TFLN, BaTiO3, and polymer-based solutions have acceptable BW
- Some may not meet the > 2 T/mm shoreline density requirement for CPO
- Require heterogeneous integration; may not achieve the reliability for CPO
- Should be suitable for pluggables with 400G serial

Silicon photonics for 400G pipes

- SiPh IMDD modulators & detectors have -3 dB BW below needs of 400G serial PAM4
- However, leverages Si fabrication and packaging & will result in high HW reliability
- Should be suitable for in the box CPO with 400G multi-λ, and/or bidirectional links
  - Lower speeds will provide improved link reliability (BER)

400G serial will leverage non-silicon solutions or use heterogeneous integration
Slower/wider silicon solutions needed for high reliability CPO solutions

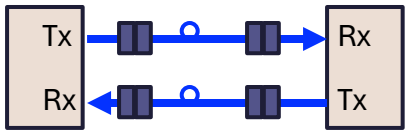
Scale-up is cost sensitive

Copper solutions are the “base” case for scale-up

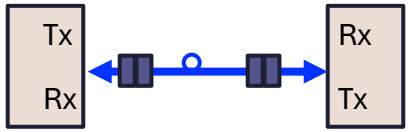
Optical solutions have traditionally been more expensive than copper

Fiber connectivity is one avenue to reduce costs

- One approach is bidirectional traffic (Tx + Rx) on a fiber
  - Reducing fiber count by 2x for single pipe links



Pair of unidirectional links



Single bidirectional link

Lower cost architectures can leverage cost reduced optical approaches

Summary

Energy efficiency is a key requirement for AI training Pods

Optical scale-up dominates the rack interconnect power

- Energy efficient solutions (CPO, LTLR) are lowest power

Scale-up interconnect will leverage Ethernet's lower layers

A pipe can carry either one or more lanes and may carry bidirectional traffic

Both hardware and link reliability is key for scale-up

- 400G serial can use non-silicon technologies and/or heterogeneous integration
- Slower/wider homogeneous silicon solutions for high reliability CPO solutions

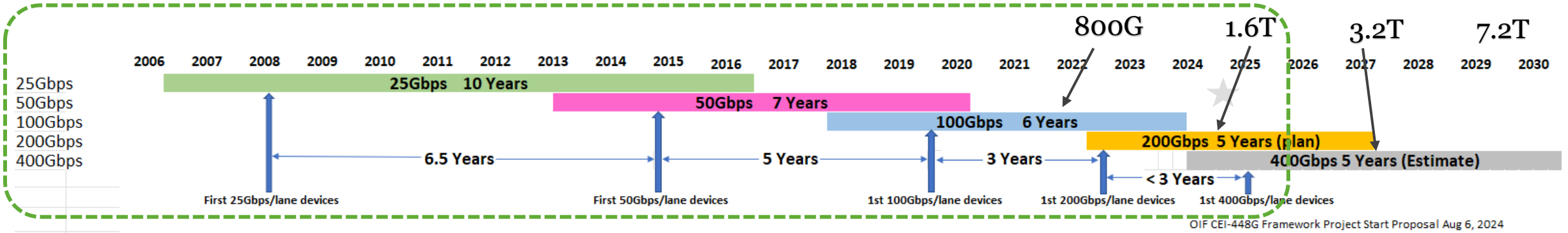
Lower cost architectures will leverage cost reduced approaches

- For example, bidirectional to reduce the amount of fiber infrastructure costs

Advances in Measurement Science

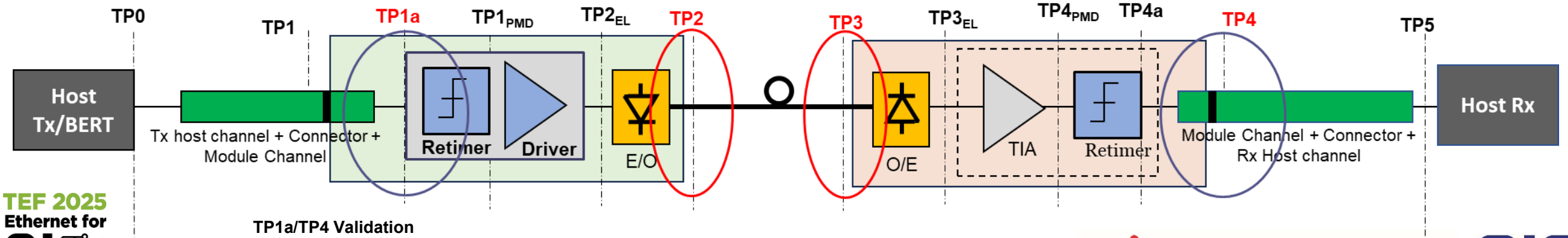
John Calvin
Senior Product Planner, Keysight Technologies

High Speed Networking Spec's -vs- First Silicon



OIF CEI-448G Framework Project Start Proposal Aug 6, 2024

Aggregate Speed	Year/ First Silicon	Single lane bit/rate	PAM modulation	Syms/UI	Signaling Fundamental	Scope BW	BW Ratio	Filter	Channel BW	Notes
200Gbps	2008	26.56	4	2	6.640	20	3	4BT	10	Open Eye Spec + CTLE
400Gbps	2014	53.125	4	2	13.281	40	3	4BT	20	RX-CTLE
800Gbps	2019	106.25	4	2	26.563	61	2.28	4BT	40	TX-FFE + RX-CTLE +RX-DFE
1.6Tbps	2022	212.5	4	2	53.125	90	1.7	4BT	67	TX-FFE + RX-CTLE +RX-FFE +RX-DFE

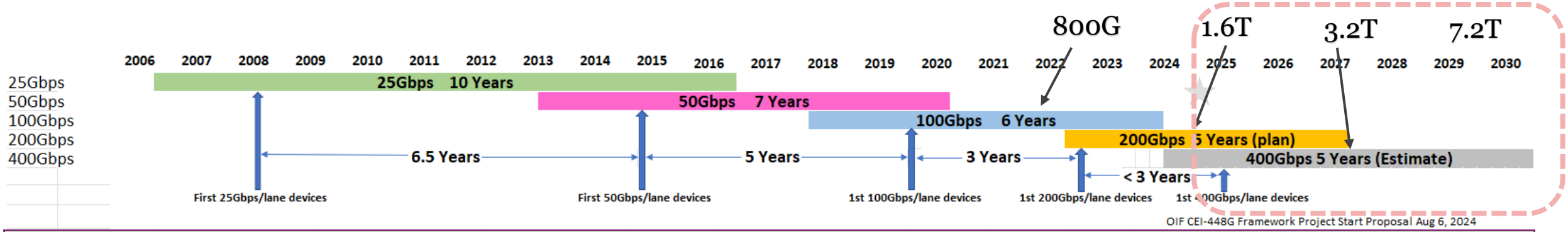


TP1a/TP4 Validation

TEF 2025 Ethernet for AI

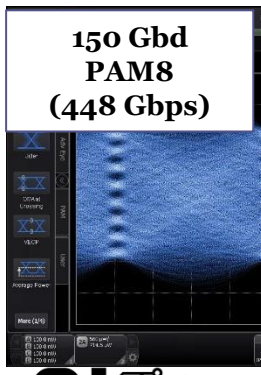
KEYSIGHT OIF

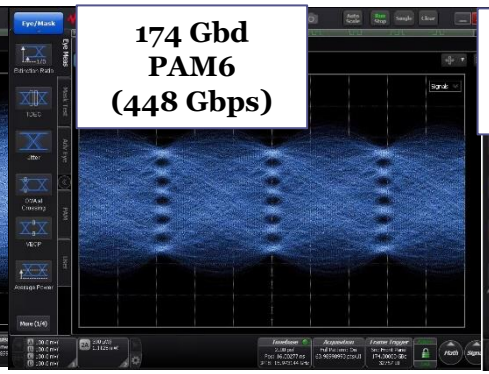
High Speed Networking Spec's -vs- Next Silicon

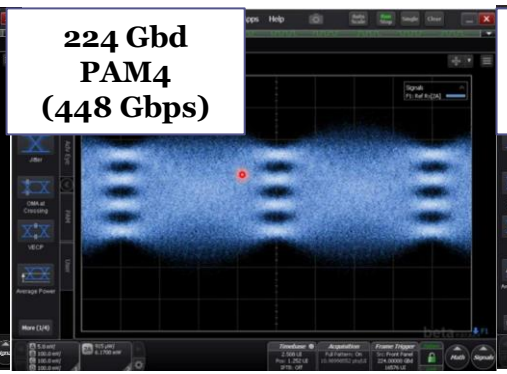


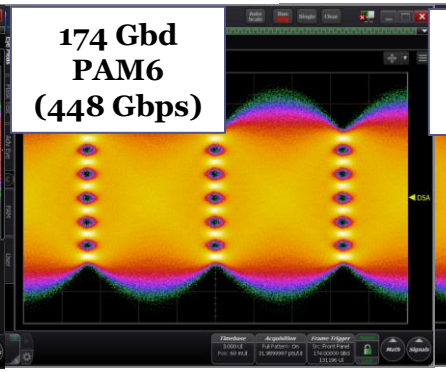
OIF CEI-448G Framework Project Start Proposal Aug 6, 2024

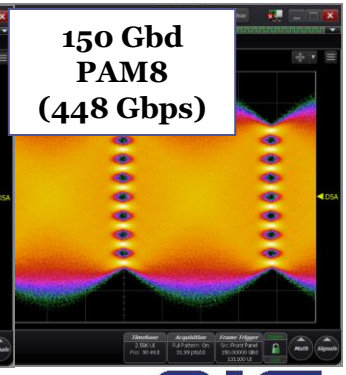
Aggregate Speed	Year/ First Silicon	Single lane bit/rate	PAM modulation	Syms/UI	Signaling Fundamental	Scope BW	BW Ratio	Filter	Channel BW	Notes
PCIe 8.0 (est)	2026	256	4	2	64.000	109	1.7	4BT	81	
3.2Tbps	2025	424	4	2	106.000	180	1.7	4BT	134	Stay the course with PAM4?
3.2Tbps	2025	424	6	2.5	84.800	127	1.5	BU	96	Switch to PAM6 ?
6.4/7.25Tbps*1	2028	848	6	2.5	169.600	212	1.25	RC	192	Expecting Raised Cosine Ref Filter.
12.8/14.5Tbps*1	2031	1696	8	3	282.667	311	1.1	RC	319	







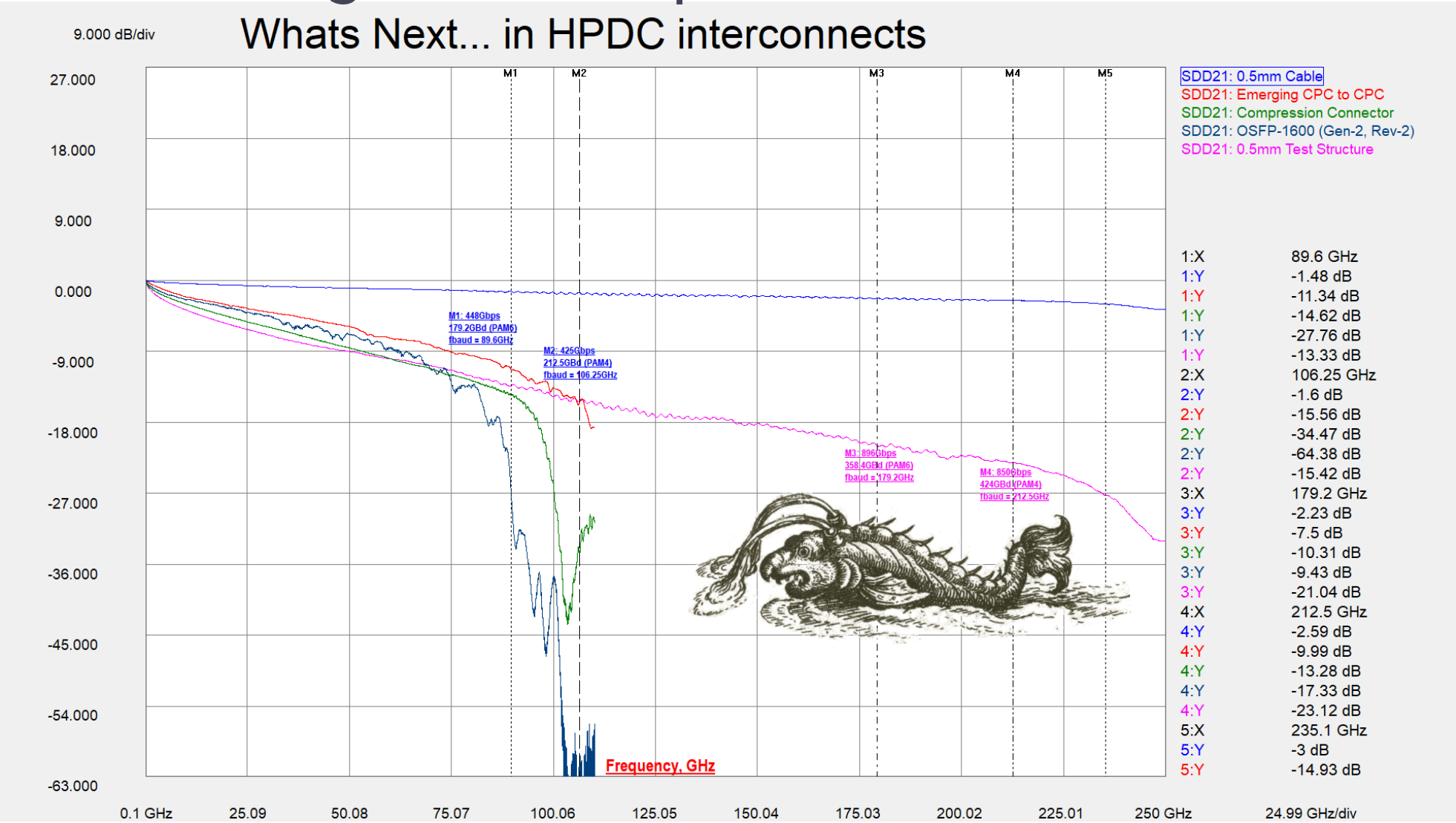




High Speed Networking.. Channel performance evolution

The edge of the electrical channel map as we know it today ends at 120GHz.

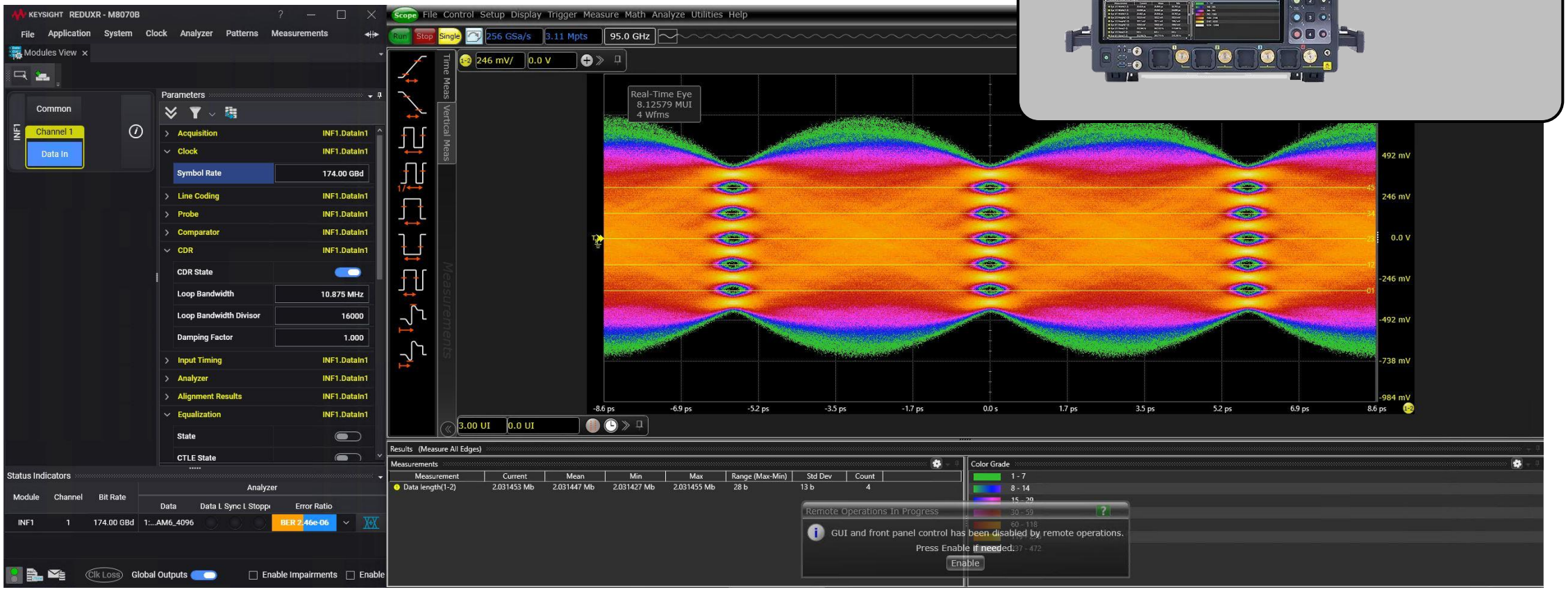
Moving into higher transmission speeds will require learning about dielectric and transmission properties for new electro-mechanical assemblies and materials.



448G Physical Error Detection

Electrical Signal Detection and BER Measurements

Realtime Oscilloscope

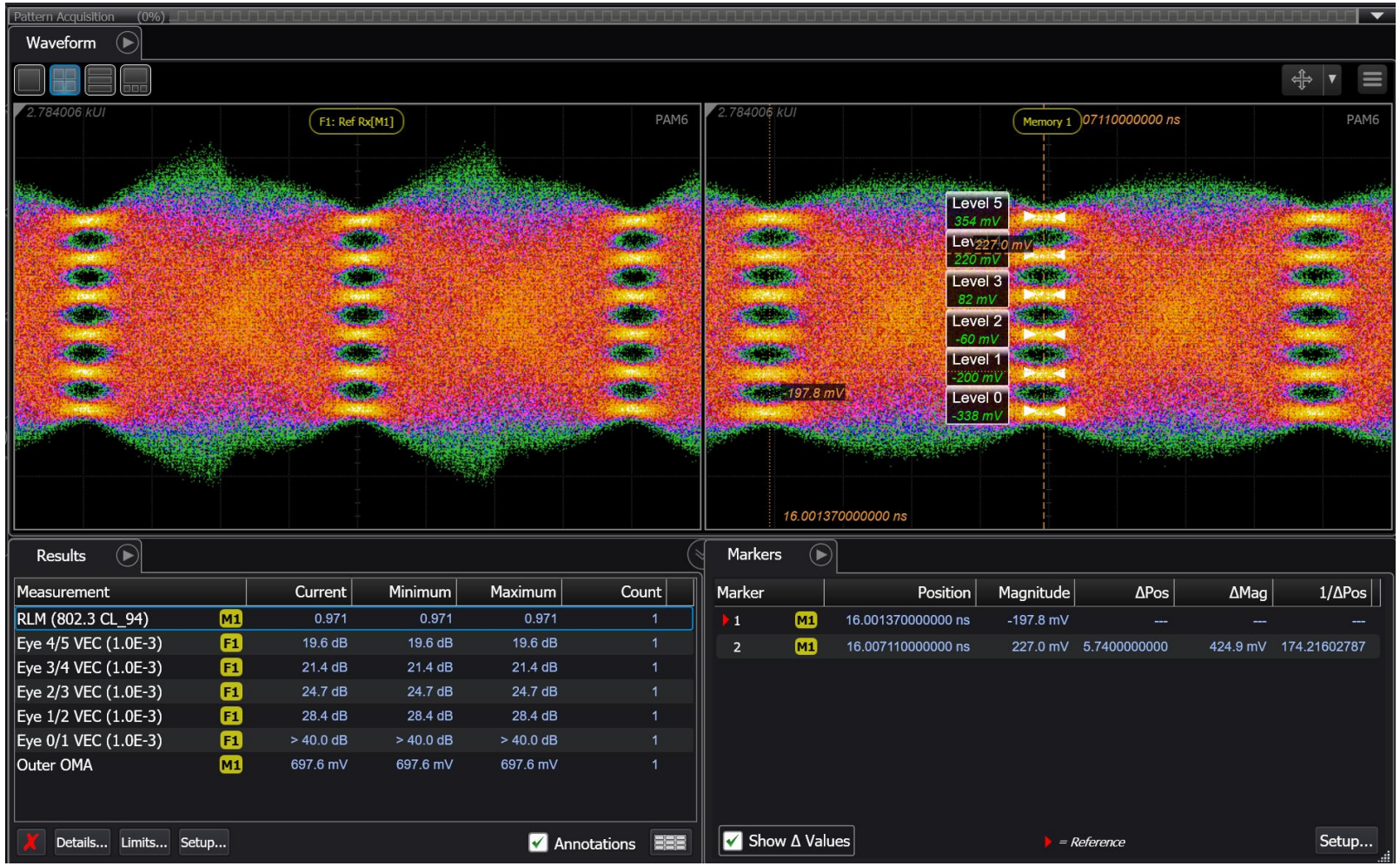


Emerging higher order measurement support

PAM6/PAM8 Analysis

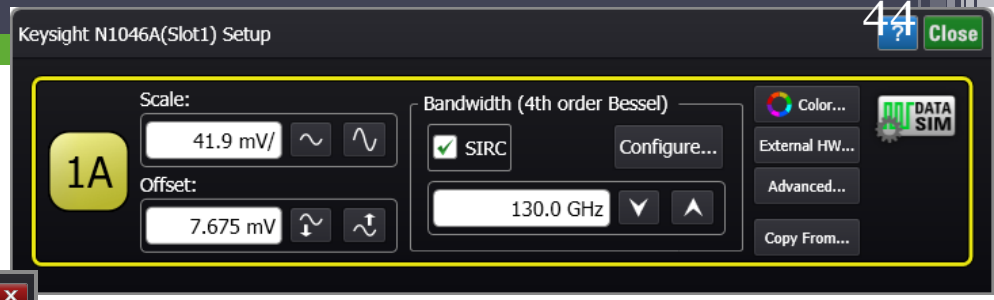
Measurements:

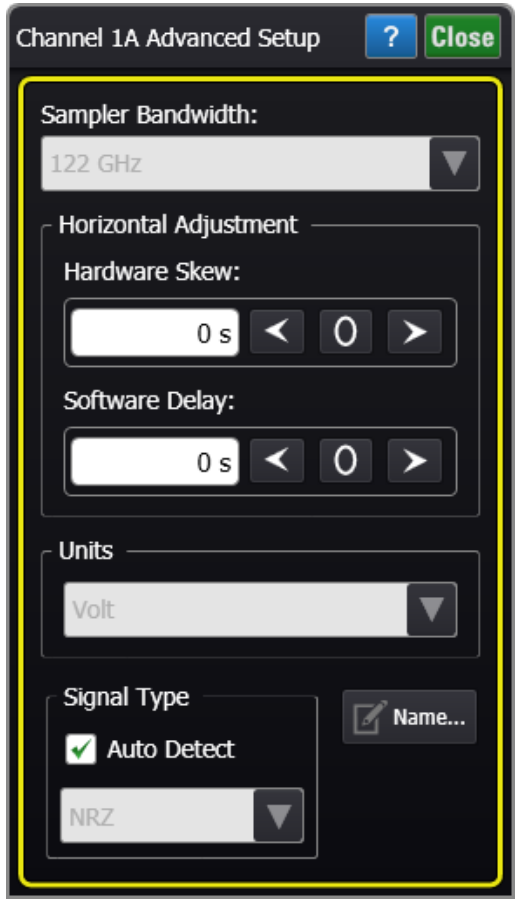
Level-Peak-Peak, RMS
Level Skews
Eye Levels
Eye Skew
Eye Height
Eye Width
Vertical Eye Closure
PAM Overshoot, Undershoot
Transition Time
Outer OMA
Outer ER
Linearity
Peak-Peak Amplitude
Tx Power Excursion
Pmax.Pmin
EECQ/TDECQ
Co-Optimized Reference Receiver Equalization



Electrical Frequency Response Plot

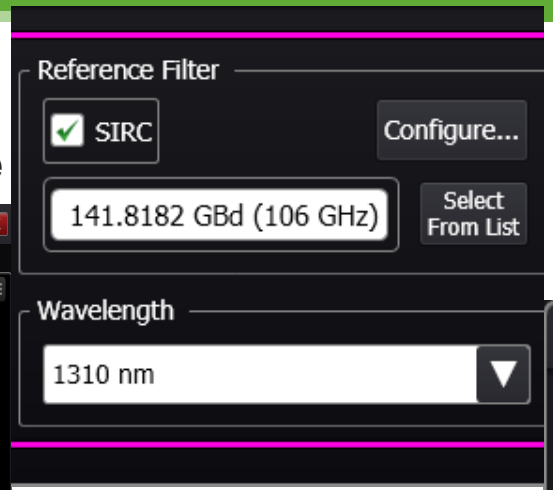
Data from ONE acquisition module – not specification, but informative

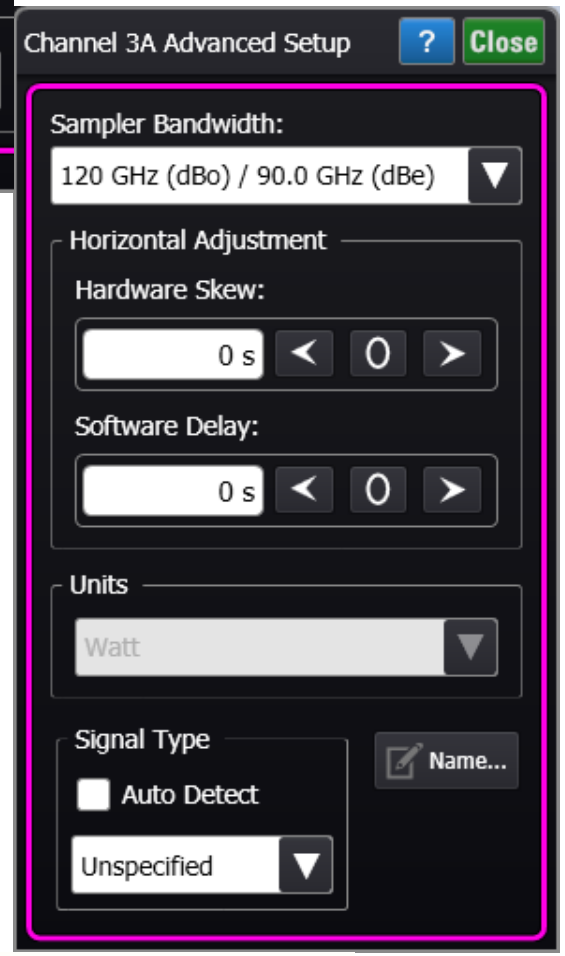




Optical Frequency Response Plot

Data from ONE acquisition module – not specification, but informative





Summary

Test instrumentation for 3.2Tbps signal generation and acquisition exist today and are not a gating limitation in determining complex issues such as modulation format.

The future of high-speed data-center transceivers and interconnects may hold several possible signaling formats to serve the various latency, radix, speed and power requirements. A single solution may not be possible.

- PAM4, PAM6, PAM8, etc.

Design requirements for channels and connectors over 100GHz are now entering mainstream with 3.2Tbps/448G. Understanding new dialectics, transmission and crosstalk properties over 100GHz will require new levels of field-solver ready engineers.

3.2Tbps/448G Signal acquisition performance will now extend across 100GHz regardless of choices of modulation order.

Flexible error detection methods will be essential for early enablement work until first silicon receivers are available.

QUESTIONS?