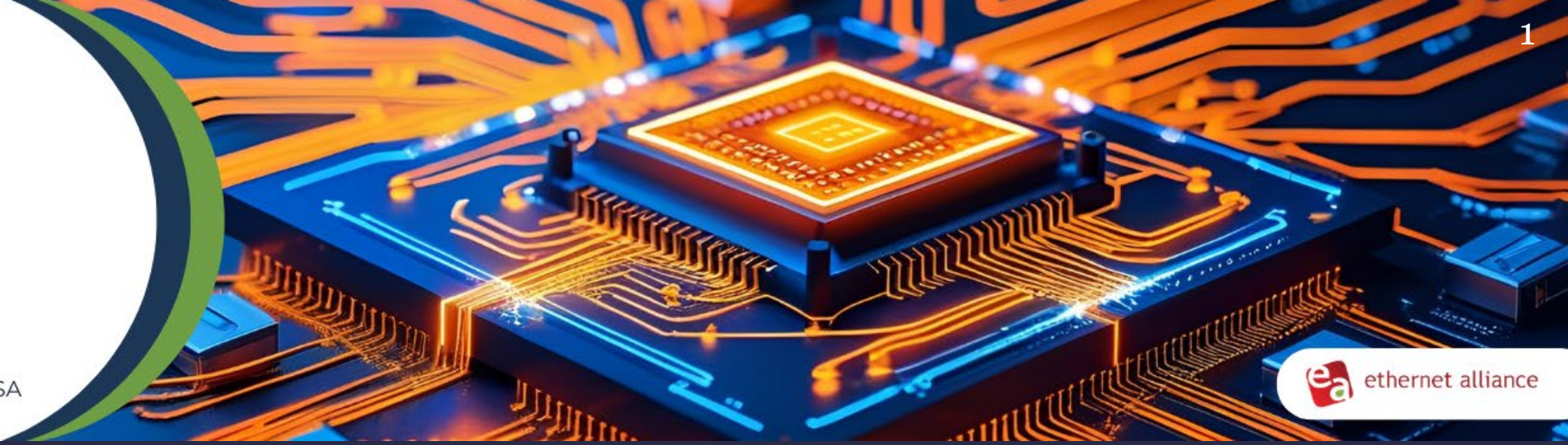


December 2-3, 2025  
Hyatt Centric Mountain View, CA, USA



# “Ethernet for AI”

John D'Ambrosia  
Chair, Ethernet Alliance TEF 2025

December 2-3, 2025





This presentation has been developed within the Ethernet Alliance, and is intended to educate and promote the exchange of information. Opinions expressed during this presentation are the views of the presenters, and should not be considered the views or positions of the Ethernet



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“At lectures, symposia, seminars, or educational courses, an individual presenting information on IEEE standards shall make it clear that his or her views should be considered the personal views of that individual rather than the formal position of IEEE.”

# What is Ethernet?



- Ethernet is an innovation brand!
- 7 Attributes
  - Native mode internet plumbing
  - High speed
  - Multi-media
  - IEEE 802.3 Standard
  - Implementations not open-sourced
  - Interoperability - Plug-n-play
  - Backwards compatibility

Source: Bob Metcalfe, Inventor of Ethernet

<http://ethernetalliance.org/tef-2013-the-future-of-ethernet-keynote/>



# Introduction



TECHNOLOGY  
EXPLORATION  
FORUM 2024

ETHERNET IN THE AGE OF AI

**TEF 2024:**  
Ethernet in the Age of AI

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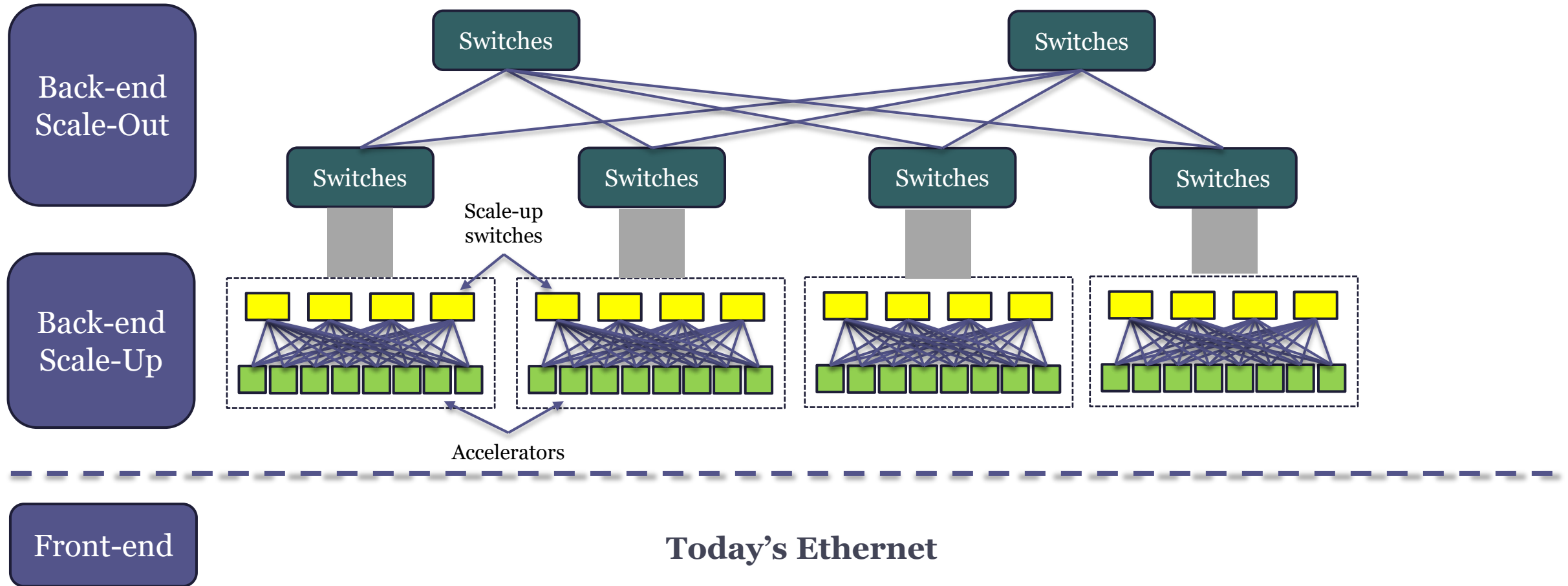
October 22-23, 2024  
Santa Clara Convention Center, CA, USA



## 2025

The year of industry wide discussions  
on 400 Gb/s signaling & technologies  
for Ethernet & AI

# AI Datacenter Network Hierarchy



A g e n d a  D a y  1	Welcome	David Rodgers, Ethernet Alliance Director of Events	9:00 AM
	Opening Comments	John D'Ambrosia, Ethernet Alliance TEF Event Chair	9:05 AM
	Keynote – “Transitioning to 400G SerDes: Key Drivers and System Design Implications for Future AI Workloads”	Halil Cirit AI Interconnect Architect, Meta	9:15 AM
	“XPU's and the Future of AI Connectivity”	Baron Fung, Dell'Oro	9:45 AM
	Break		10:15 AM
	Panel #1 – “400 Gb/s Signaling for AI Networks From a System Perspective”	Moderator: Alan Weckel, 650 Group <ul style="list-style-type: none"> <li>• Gary Nicholl, Cisco, “CMIS – The management interface that ties everything together for AI”</li> <li>• Brian Welch, Cisco, “Building systems for AI deployments”</li> <li>• Arihant Jain, Arista, “AI Scale-Out Network Designs and Interconnects”</li> </ul>	10:30 AM
	Lunch		12:00 PM
	“Ultra Ethernet: AI Evolution & Insights for 400G”	Adee Ran, Cisco	1:00 PM
	Panel #2 – “The Path To 448G in Support of Next Generation AI”	Moderator, Nathan Tracy, OIF Board Member, TE Connectivity <ul style="list-style-type: none"> <li>• Cathy Liu, Broadcom, “Electrical Channel Characteristics”</li> <li>• Mike Li, Altera (an Intel Company), “Electrical Channel Modulation”</li> <li>• Jeff Hutchins, Ranovus, “Does optics have what is needed for scale-up link?”</li> <li>• John Calvin, Keysight Technologies, “Test and Measurement”</li> </ul>	1:30 PM
	Break		3:00 PM
	Panel #3 – “FEC and 400 Gb/s Signaling for AI Networks”	Moderator: Alan Weckel, 650 Group <ul style="list-style-type: none"> <li>• Xiang He, Huawei, “FEC for 448G: Can Today's FEC Survive Tomorrow's Modulation?”</li> <li>• Tony Chan Carusone, Alphawave Semi, “Channel-Aware Modulation and FEC Selection for 400G+ Ethernet”</li> <li>• Adam Healey, Broadcom, “Benefits and limitations of inner error-correcting codes for 400 Gb/s per lane electrical links”</li> </ul>	3:30 PM
	Break for Day		5:00 PM
	Reception		5:30 PM

A g e n d a  D a y  2	Opening Comments	Opening Comments - John D'Ambrosia, Ethernet Alliance TEF Event Chair	9:00 AM
	Panel #4 <b>"400 Gb/s Optics for AI Networks"</b>	Moderator: Vlad Kozlov, LightCounting <ul style="list-style-type: none"> <li>Gilad Shainer, Nvidia, "Co-Packaged Silicon Photonics Switches for Gigawatt AI Factories"</li> <li>Jose Castro, Panduit, "Enabling Massive Scale-Out AI Networks with Ethernet and Optical Lane Breakouts"</li> <li>Dr. Naim Ben-Hamida, Ciena, "Ethernet for AI"</li> </ul>	9:05 AM
	Break		10:35 AM
	Panel #5 <b>"Copper Interconnect for 400 Gb/s Signaling for AI Networks"</b>	Moderator: Lisa Huff, DC Tech Analysis <ul style="list-style-type: none"> <li>Kasthuri Sankar Damodharan, Amphenol, "Solving 400Gb/s at the Speed of Interconnect"</li> <li>Ashika Pandankeril Shaji, TE Connectivity, "400G/lane Interconnects for AI: Channel Feasibility, Reach Extension, and Early Measurement Results"</li> <li>Augusto Panella, Molex, "Copper Backplane Considerations for 400G Signaling"</li> </ul>	10:45 AM
	Lunch		12:00 PM
	<b>SNIA Storage for AI Efforts</b>	Tom Palkert, Samtec, Chair of the SNIA/SFF Transceivers Subgroup	1:00 PM
	Panel #6 <b>"400 Gb/s Electrical Signaling for AI Networks"</b>	Moderator: Lisa Huff, DC Tech Analysis <ul style="list-style-type: none"> <li>Ayal Shoval, Synopsys, "Proposed Enhancements to COM: Addressing RLM Sensitivity in Next-Generation Ethernet Designs"</li> <li>Hadrien Louchet, Keysight, "Advancing 448G Signal Generation and Analysis with Modern Test &amp; Measurement Solutions"</li> <li>Jim Hsieh, MediaTek, "Unveiling Bottlenecks in Measured Co-Packaged Copper Channels: Sensitivity Analysis at 75–90 GBd for PAM6/8"</li> <li>Bijan Nowroozi, Lightmatter, "Modularity at the Package Edge: Composable Interconnect for 400 Gb/s/Lane AI Systems"</li> </ul>	1:30 PM
	Break		3:00 PM
	<b>"Ethernet for AI Isn't Just Evolving — It's Exploding"</b>	John D'Ambrosia, Chair, IEEE 802.3 NEA "Ethernet for AI" Assessment, Futurewei	3:15 PM
	<b>"Defining 400bps per Lane Electrical and Optical Signaling for Ethernet"</b>	Kent Lusted, Champion, IEEE 802.3 Mar 2026 CFI - 400 Gb/s Signaling Ethernet Project, Synopsys	3:50 PM
	Wrap-up	John D'Ambrosia, Ethernet Alliance TEF Event Chair	4:30 PM
	End of Day		4:45 PM

# Introductions



Kent Lusted  
IEEE 802.3  
400 Gbps/Lane  
CFI Champion  
Synopsys



David Law  
IEEE 802.3 Chair  
HPE



John D'Ambrosia  
IEEE 802.3  
3.2 TbE  
CFI Champion  
Futurewei



James Gilb  
IEEE 802 Chair  
General Atomics  
Aeronautical Systems,  
Inc.



Adam Healey  
IEEE 802.3 Vice Chair  
Broadcom



# Note of Thanks

- Our Moderators
  - Lisa Huff - DC Tech Analysis
  - Alan Weckel - 650 Group
  - Vlad Kozlov - LightCounting
  
- Our Keynote
  - Halil Cirit, Meta
  
- And all of our Speakers

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